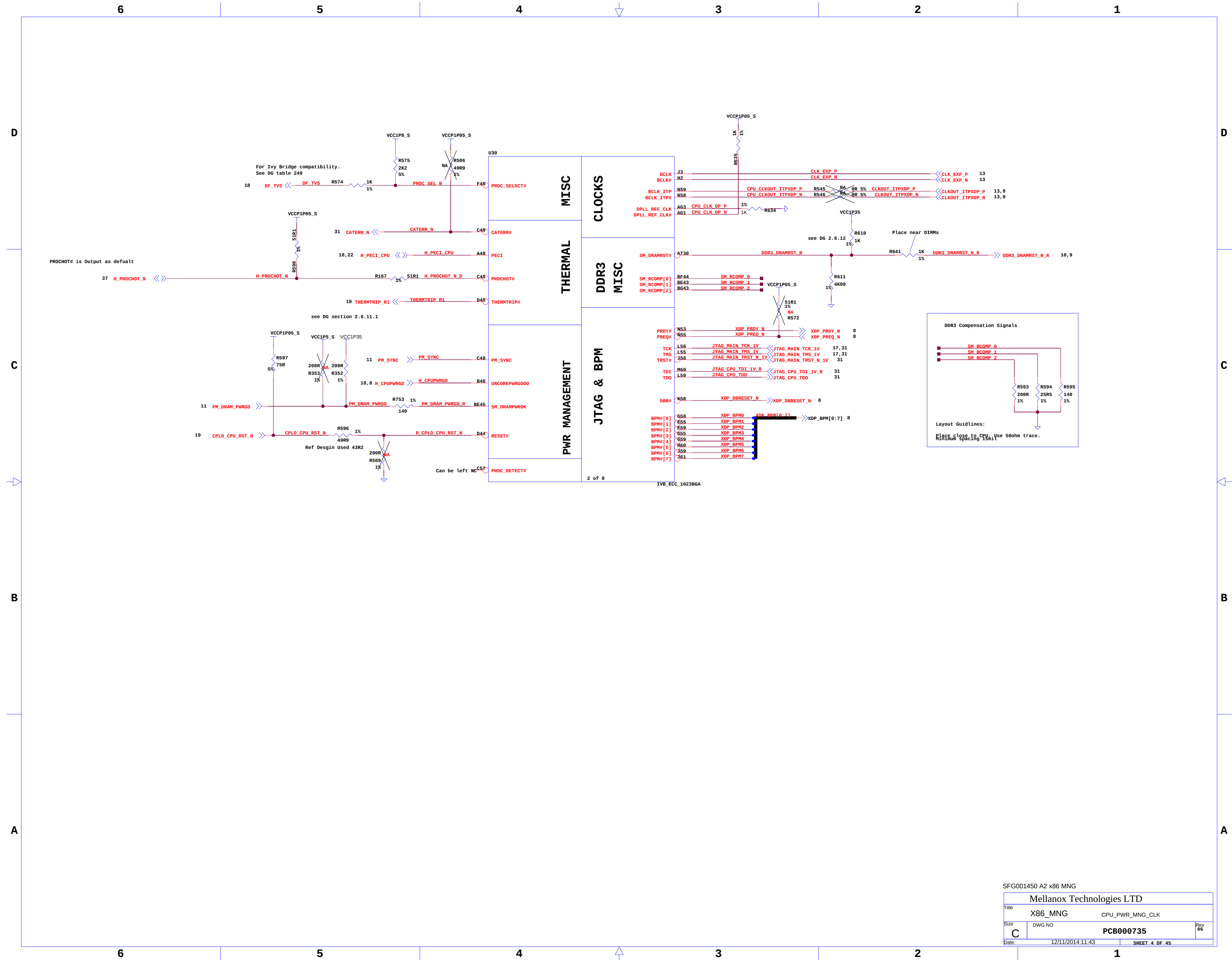






6

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D

D

C

C

B

B

A

A

GFX disabled according to 2.3.8 in DG

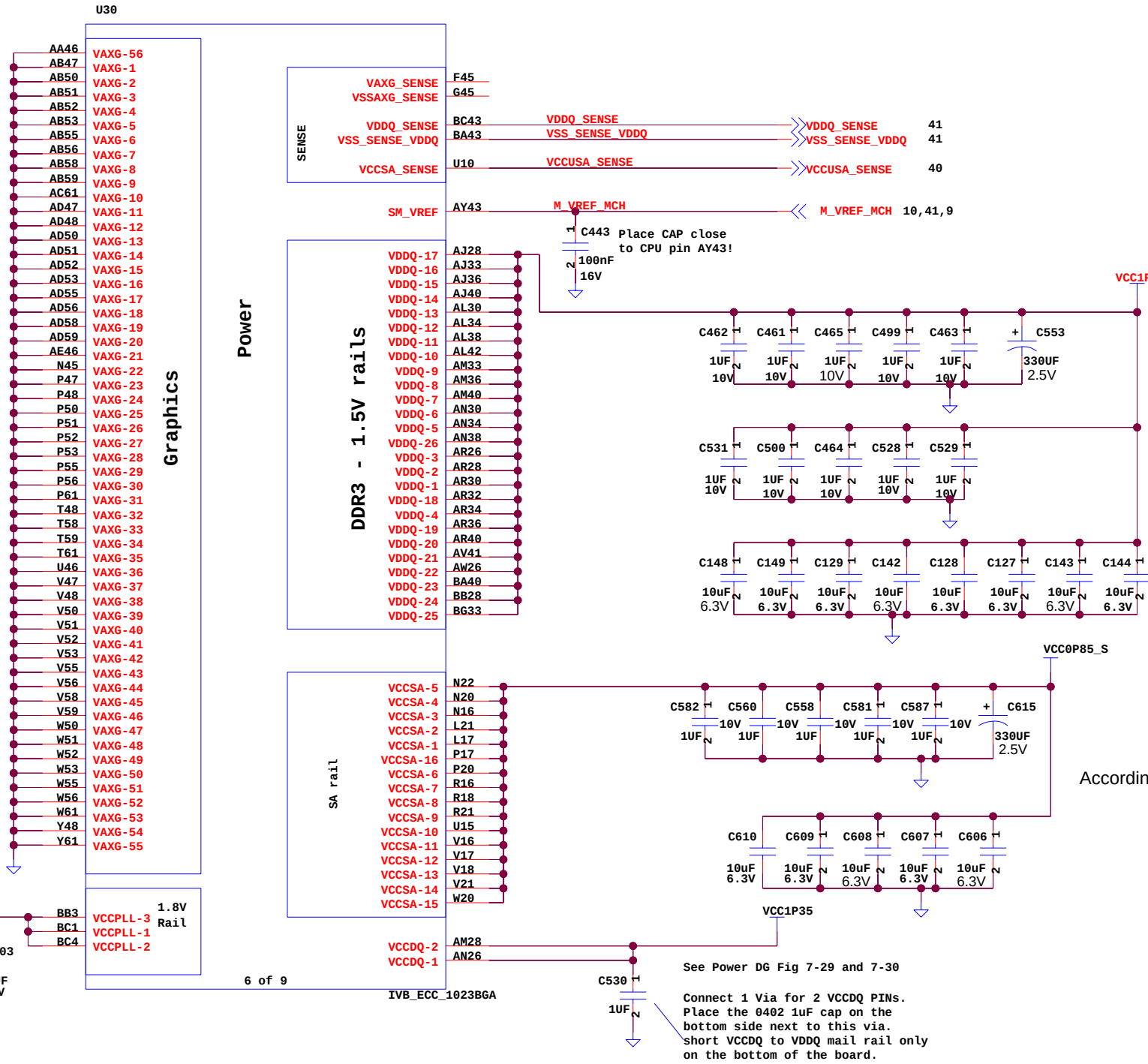
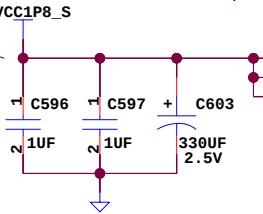
Trace Impedance: 27-33 Ohm
See layout instructions in PWR DG Section 2.7 for all sense signals

According to Power DG table 7-11

According to Power DG table 7-9

According to Power DG table 7-5

Layout Guidelines: PLL as generated plane, connect to main plain using vias.



See Power DG Fig 7-29 and 7-30
Connect 1 Via for 2 VCCDQ PINs.
Place the 0402 1uF cap on the bottom side next to this via.
Short VCCDQ to VDDQ rail only on the bottom of the board.

SFG001450 A2 x86 MNG			
Mellanox Technologies LTD			
Title	X86_MNG CPU_Power_1		
Size	DWG NO	PCB000735	Rev 06
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6

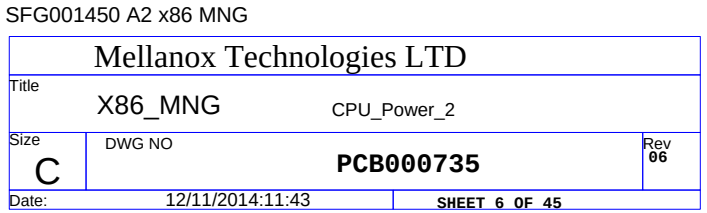
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D

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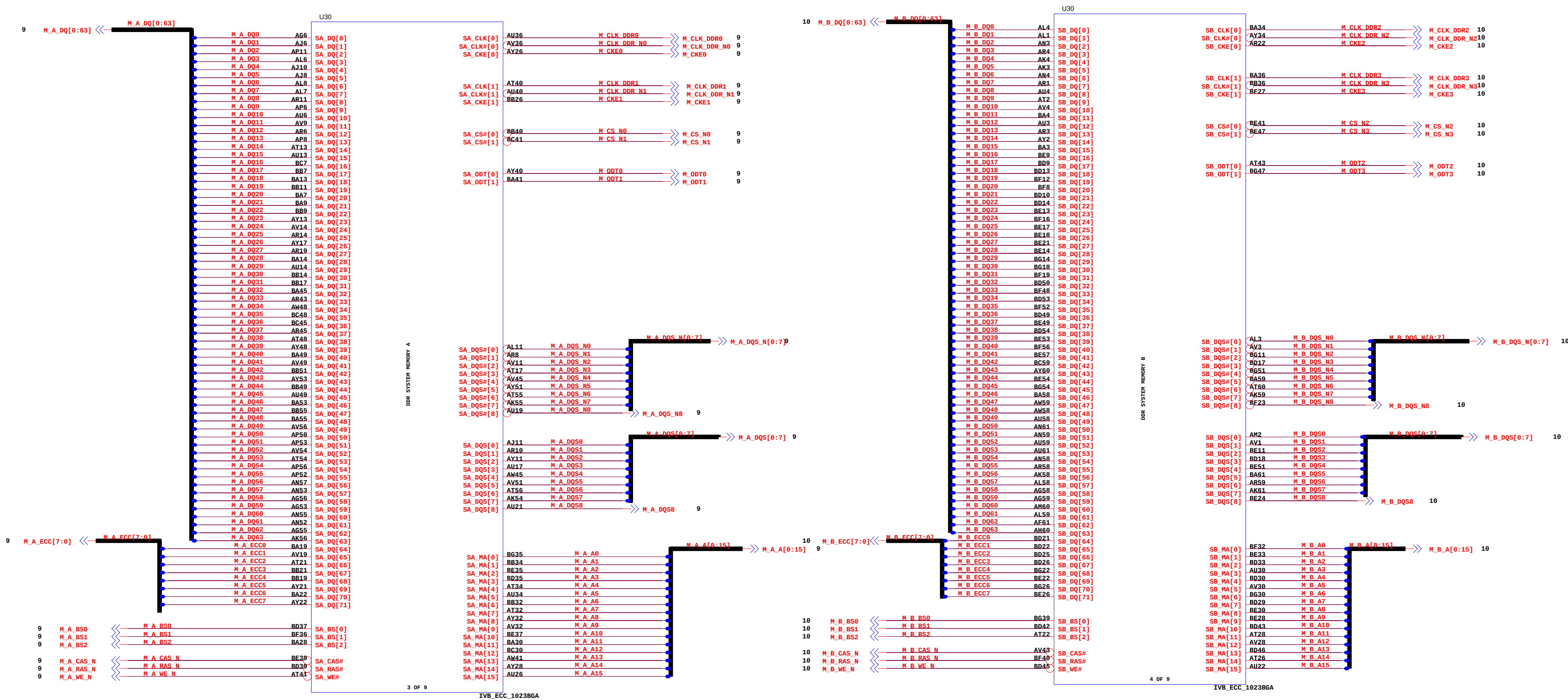
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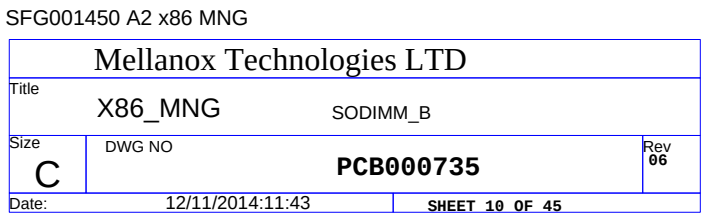
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C

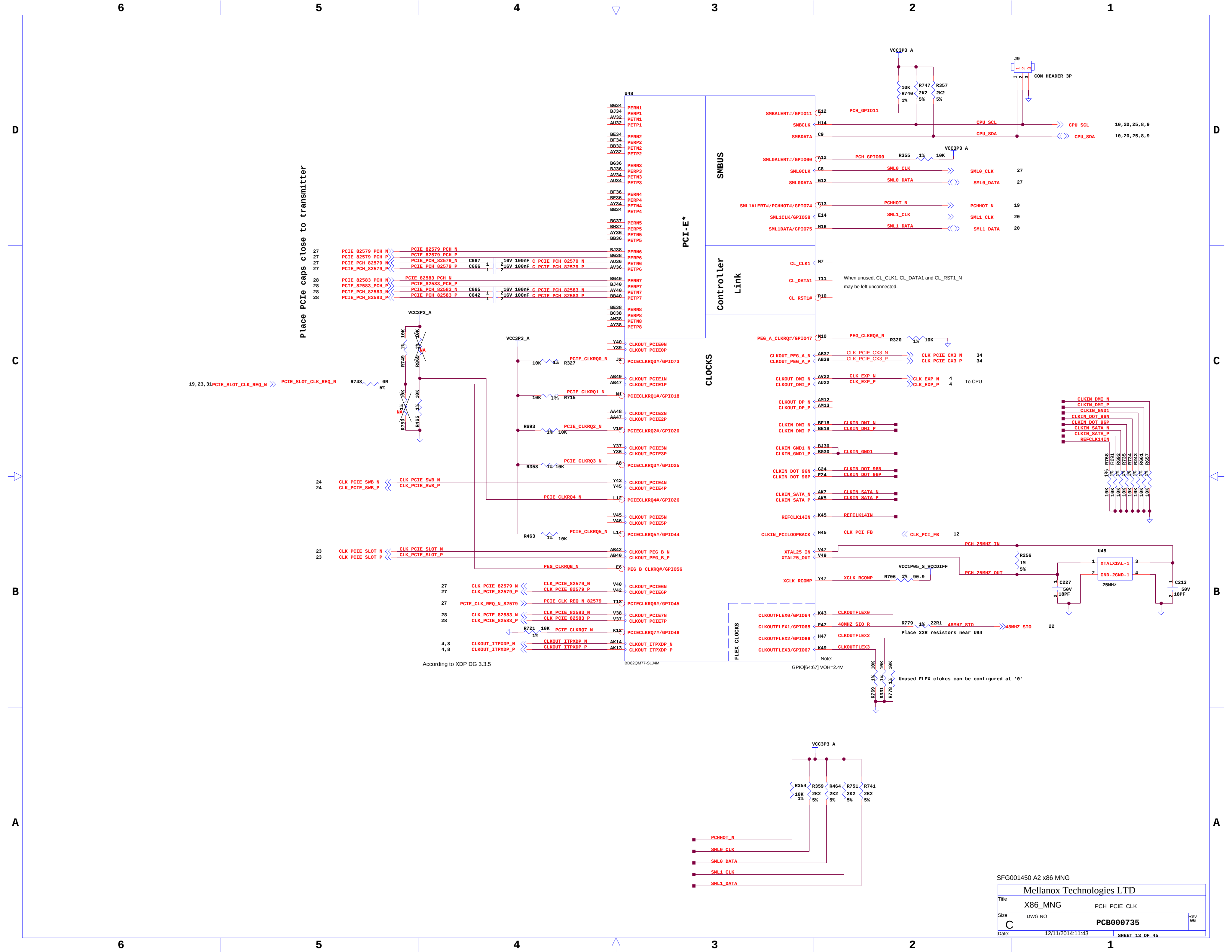
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A





SFG001450 A2 x86 MNG



D

C

B

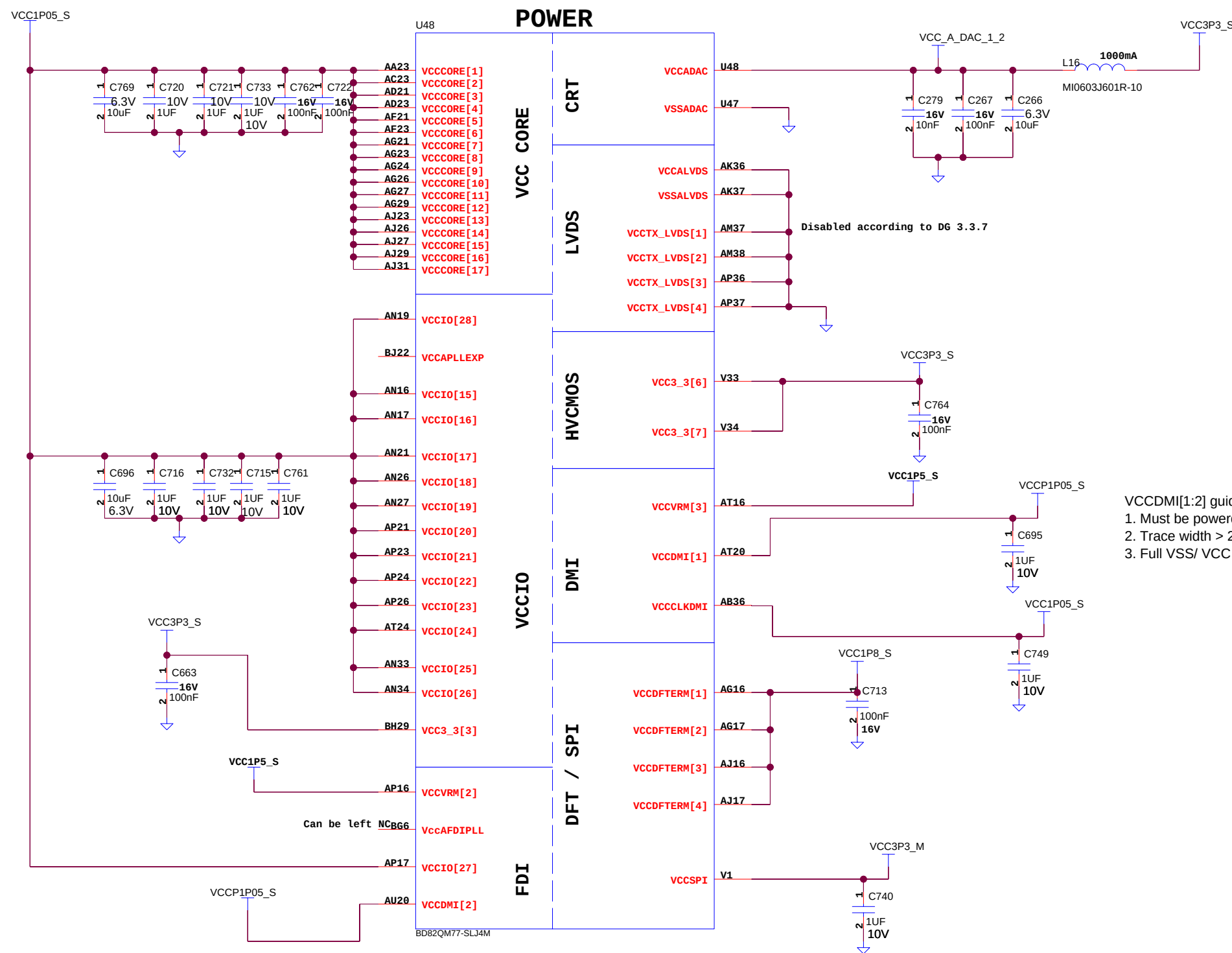
A

D

C

B

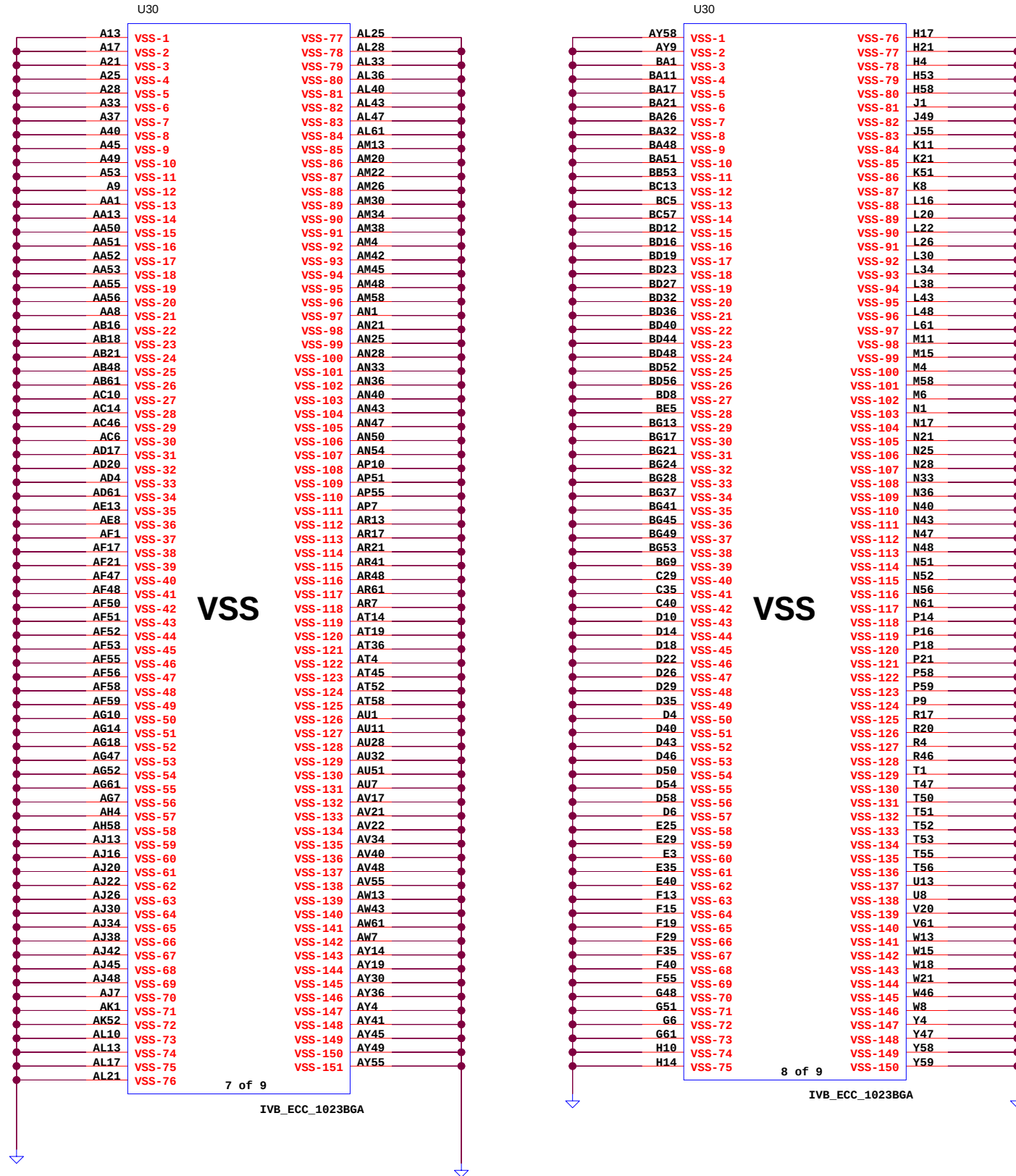
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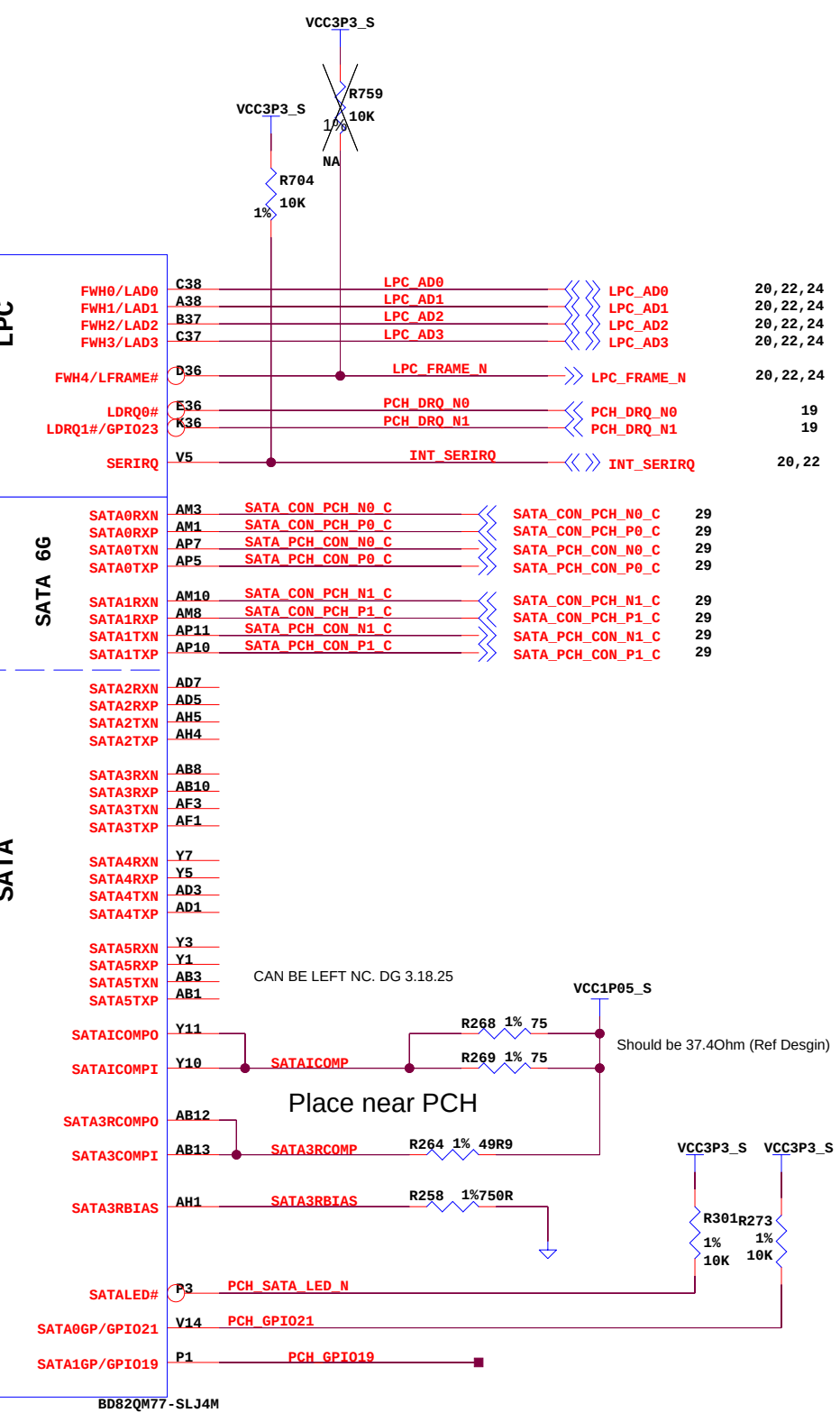
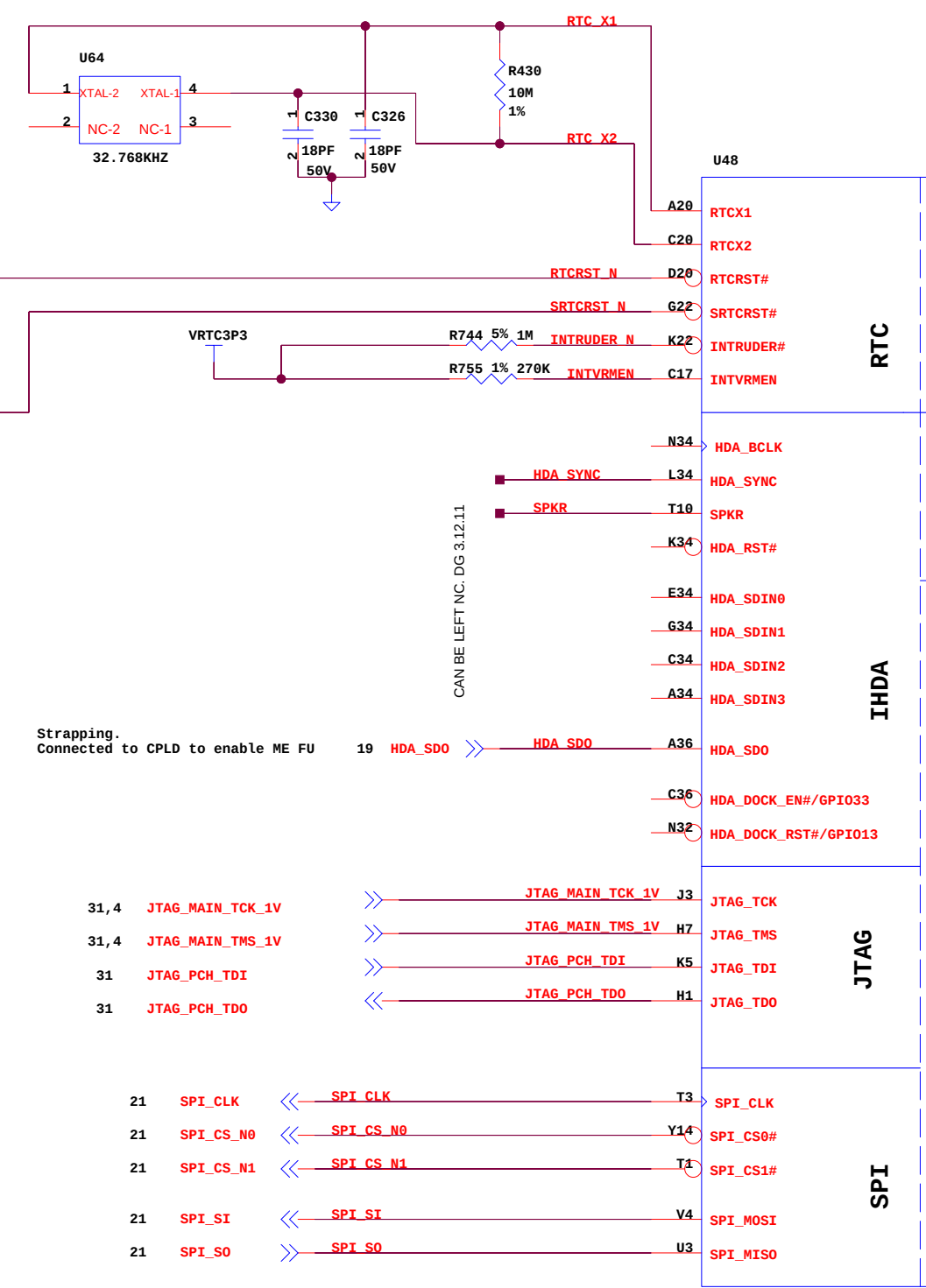
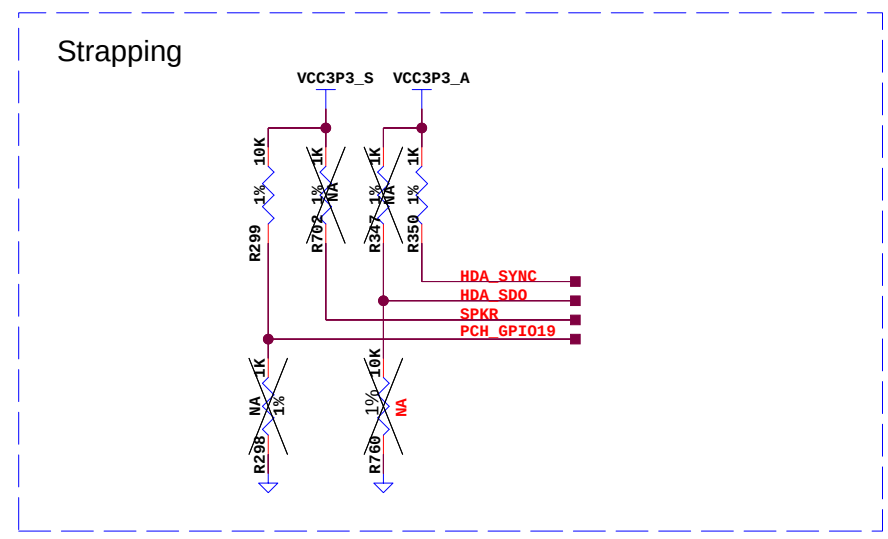
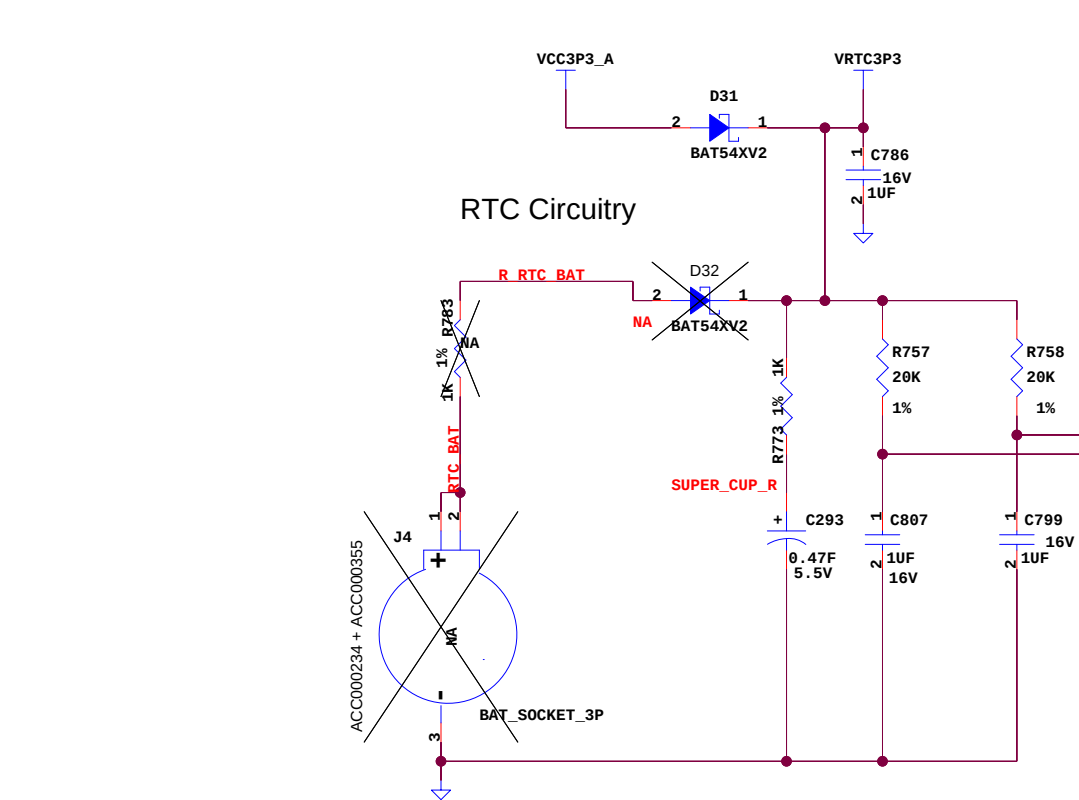
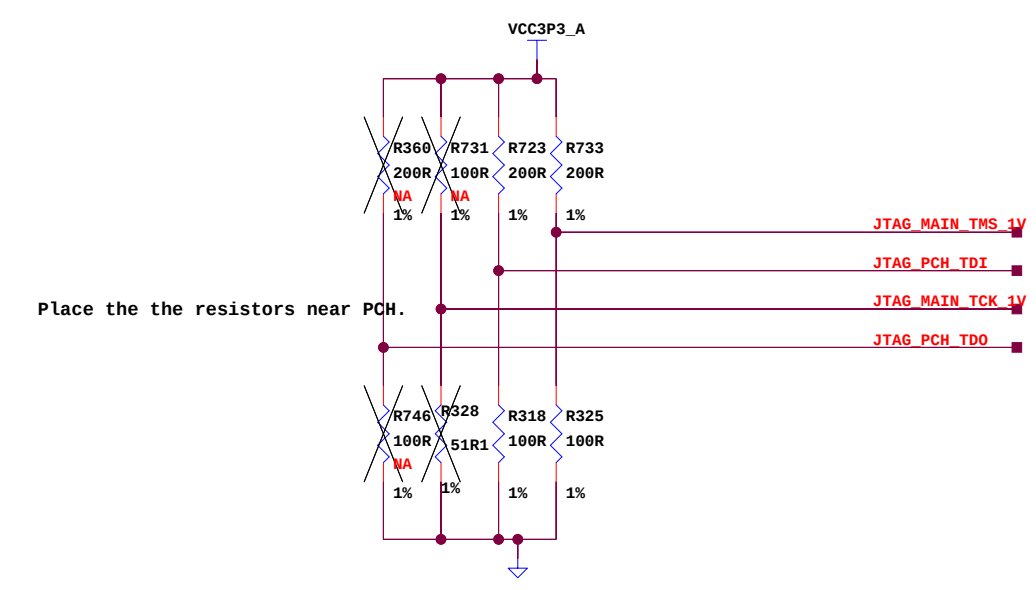


SFG001450 A2 x86 MNG

Mellanox Technologies LTD			
Title	X86_MNG		PCH_POWER1
Size	DWG NO	PCB000735	Rev 06
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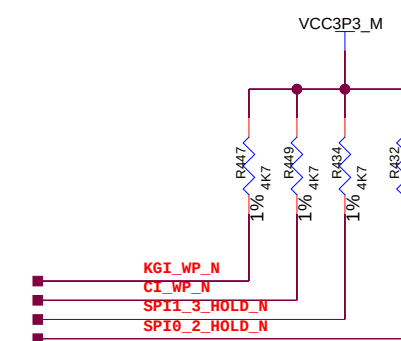
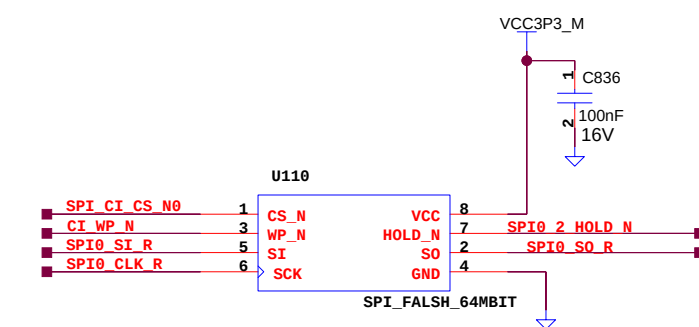
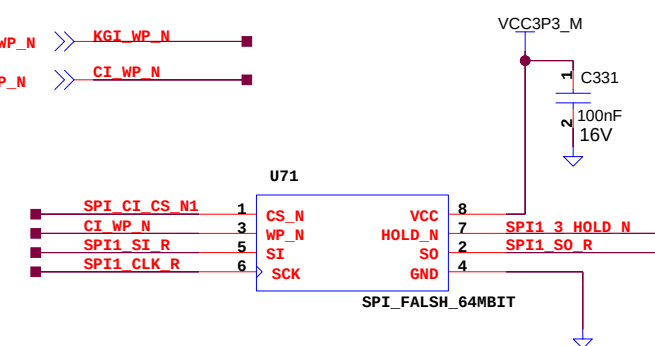
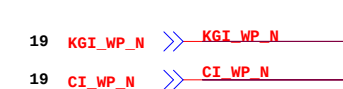
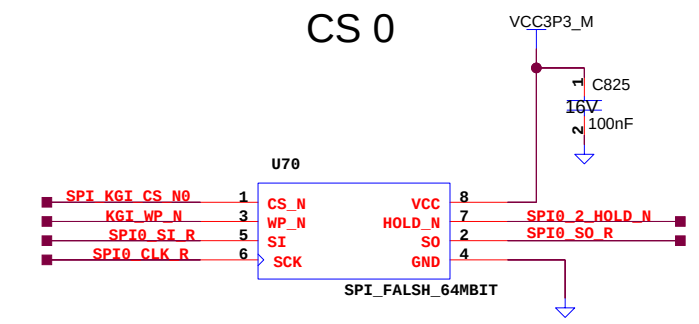
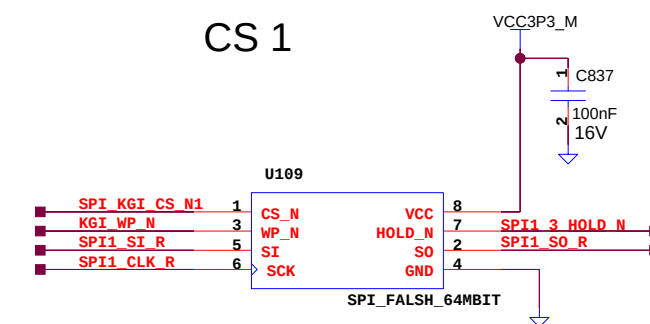
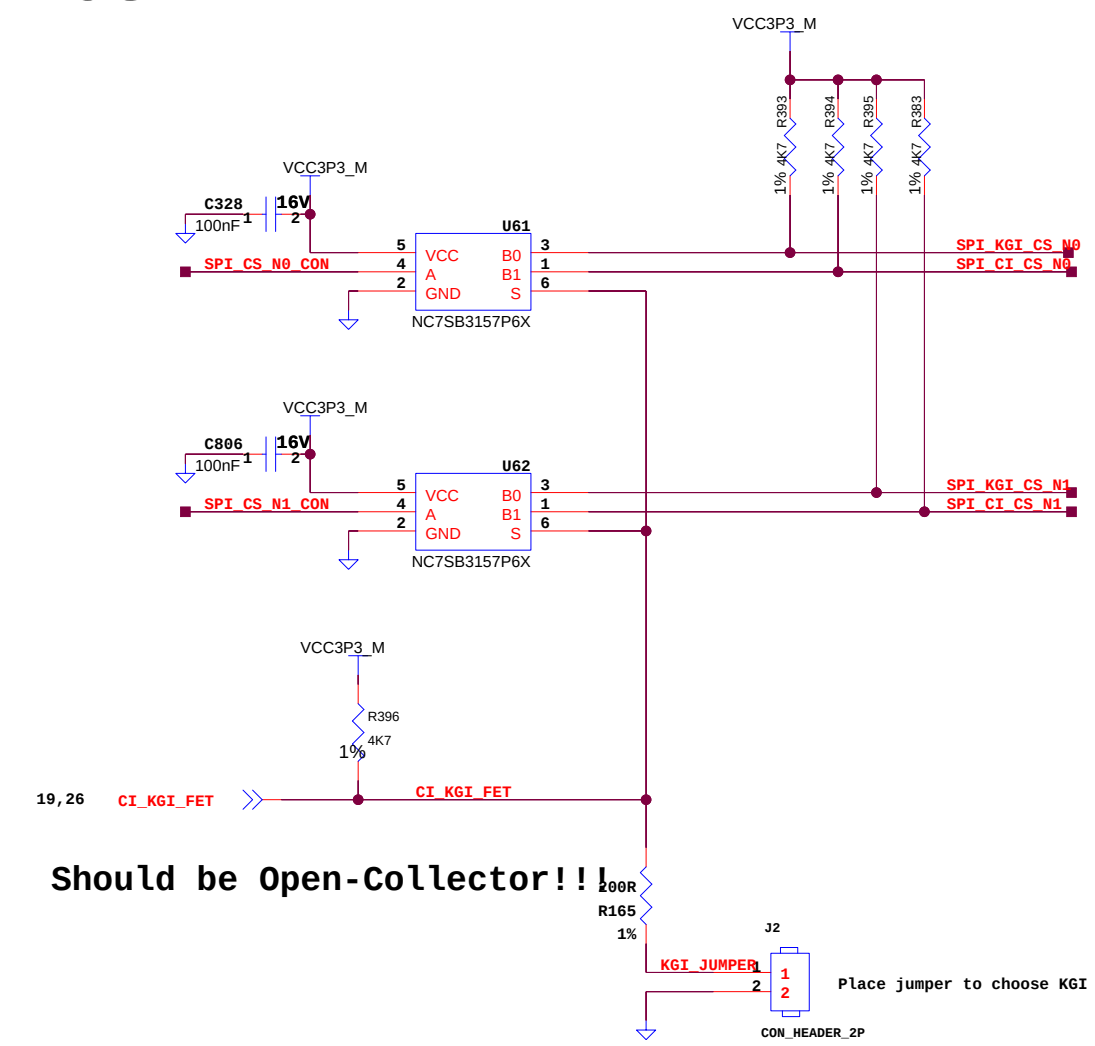
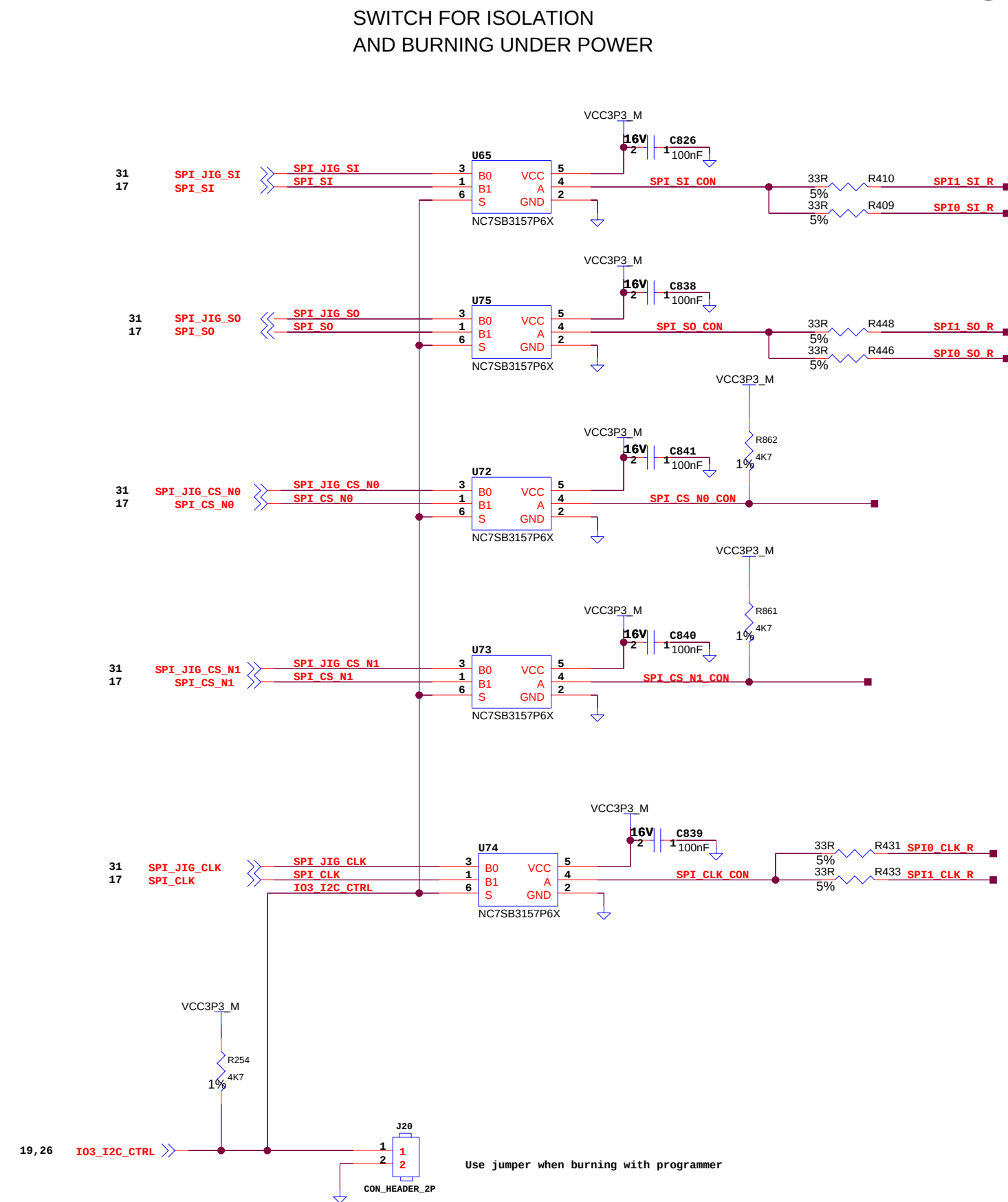
CPU





Internal PU on LAD[0:3], LDRQ0#, LDRQ1#

See Layout guidelines



Known Good Image

Current Image

D

D

C

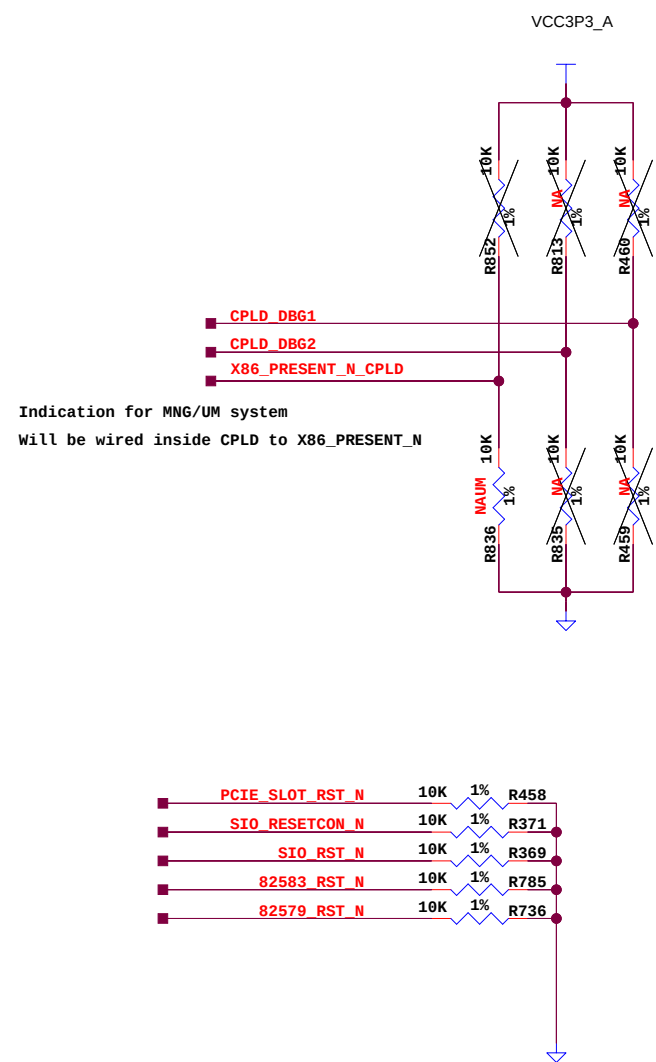
C

B

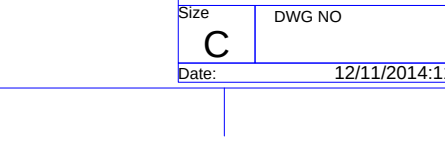
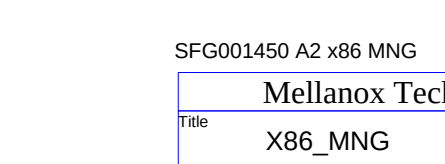
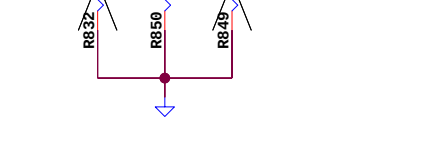
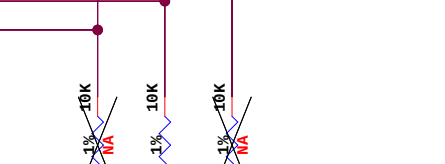
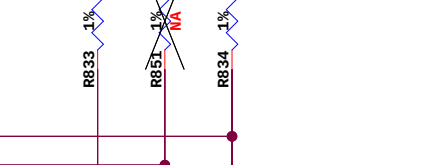
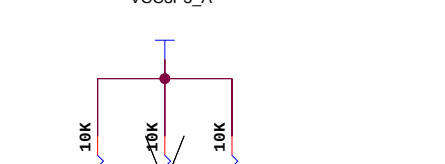
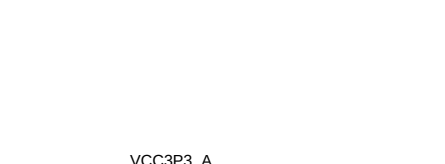
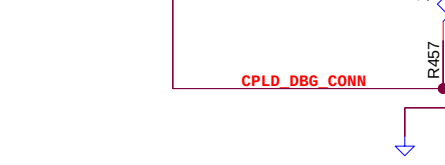
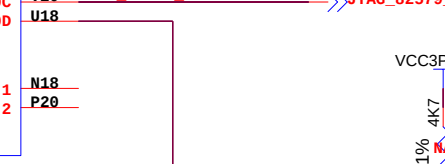
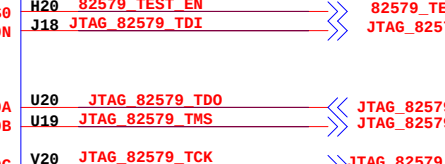
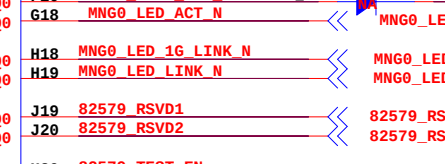
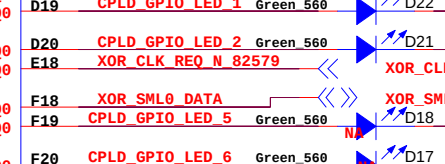
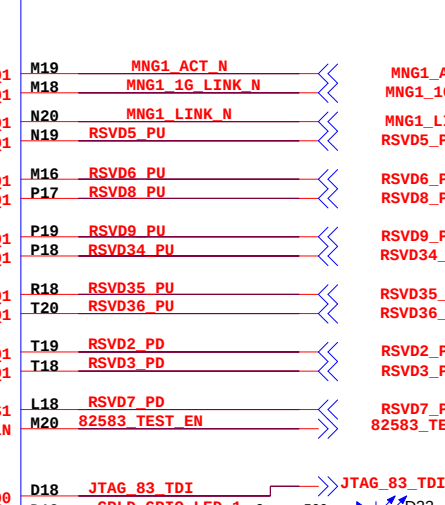
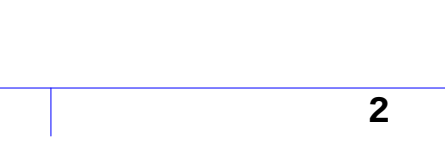
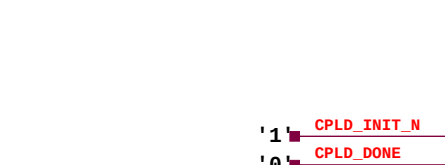
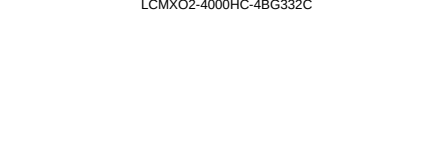
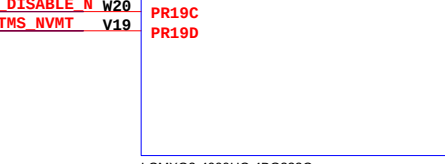
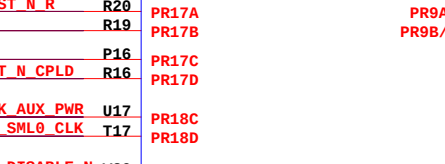
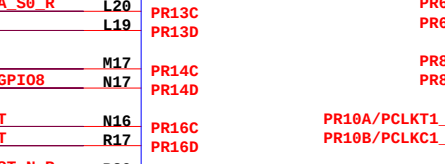
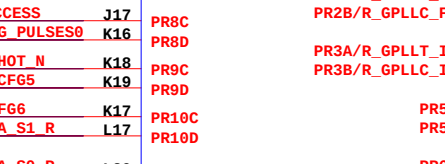
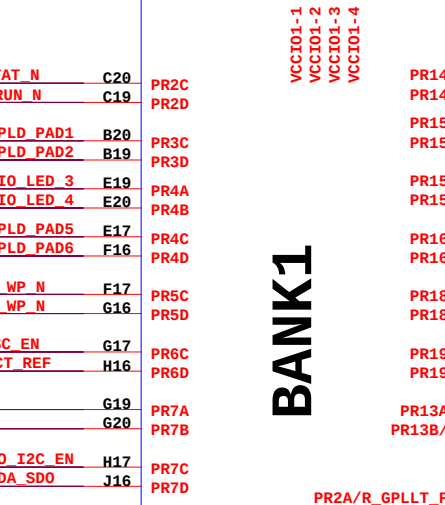
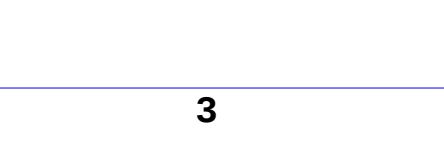
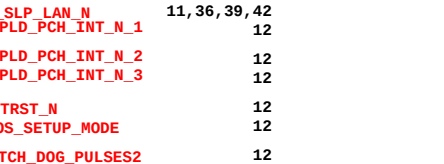
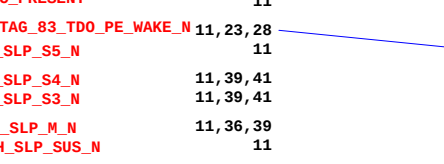
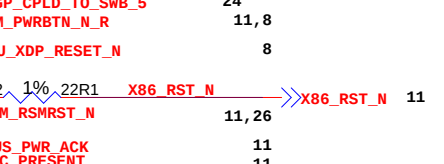
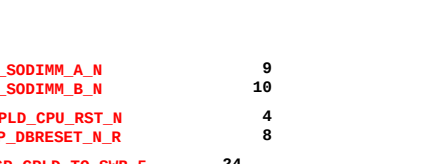
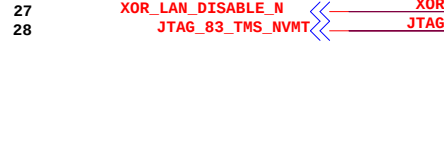
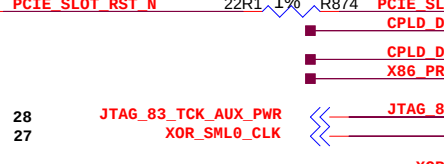
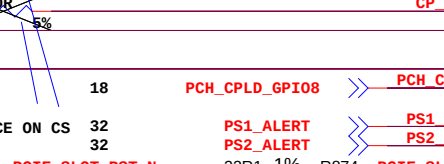
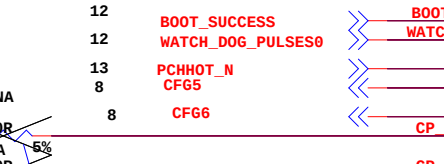
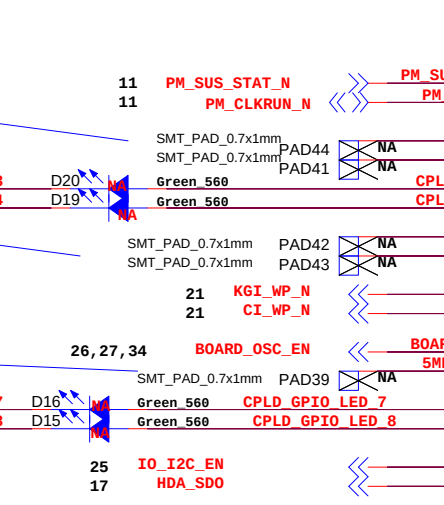
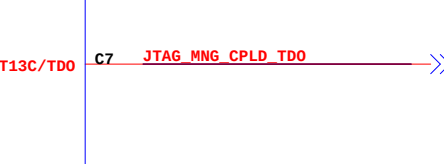
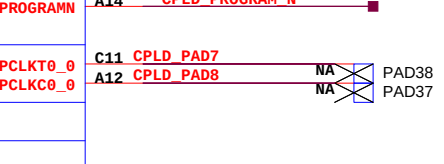
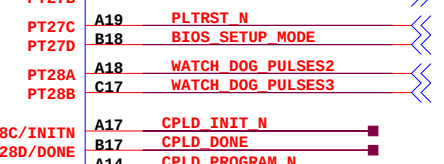
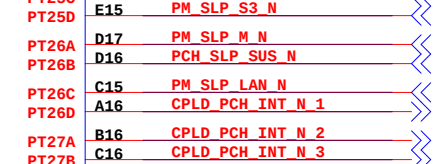
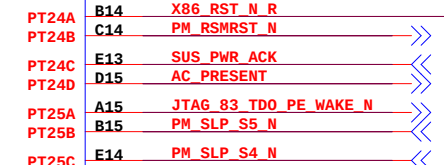
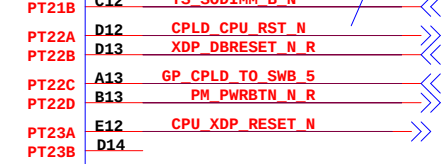
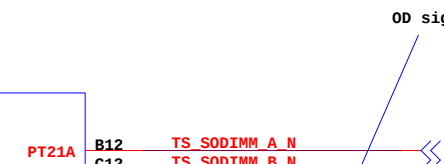
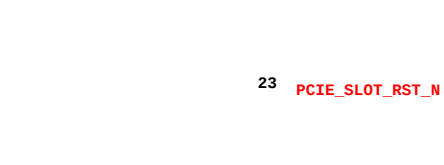
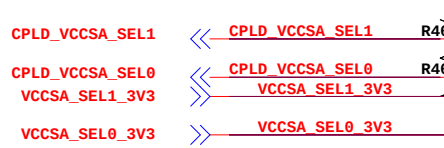
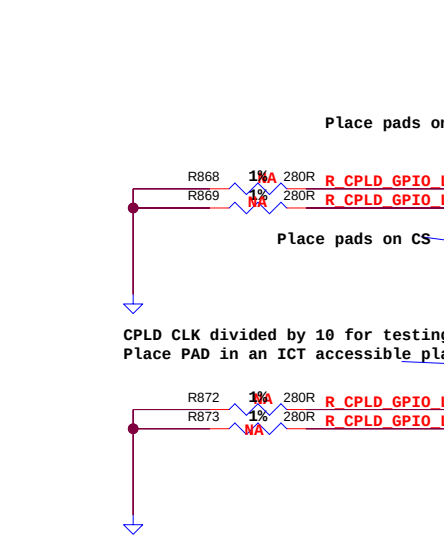
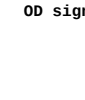
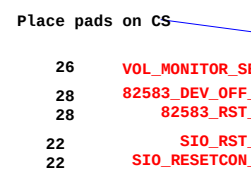
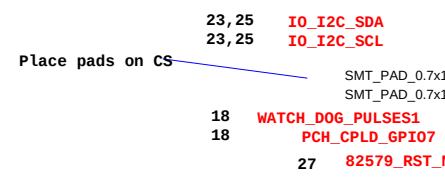
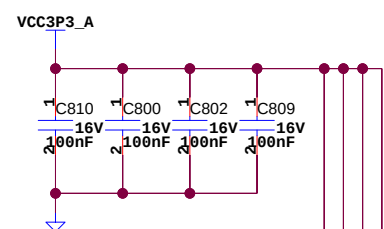
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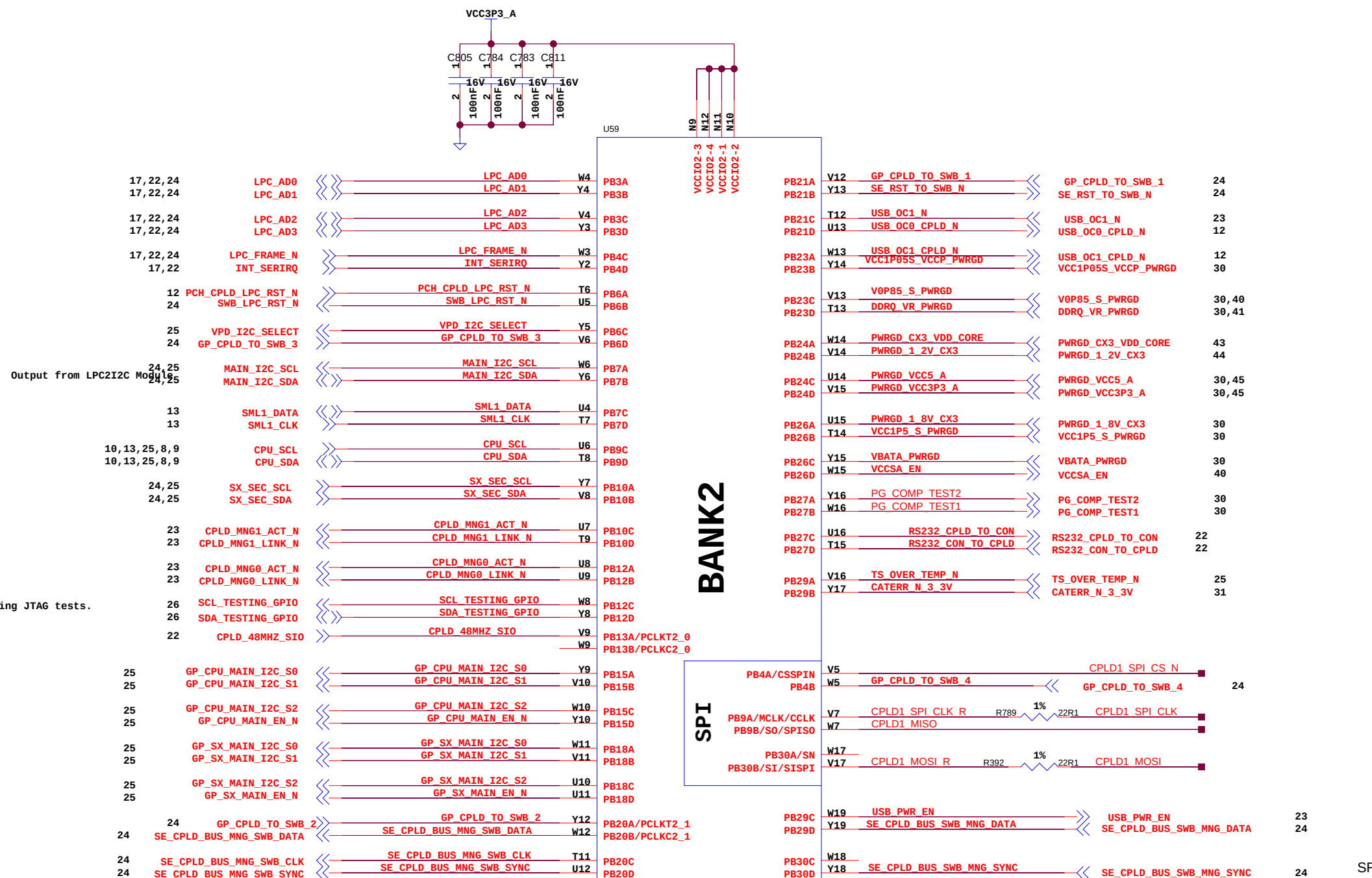
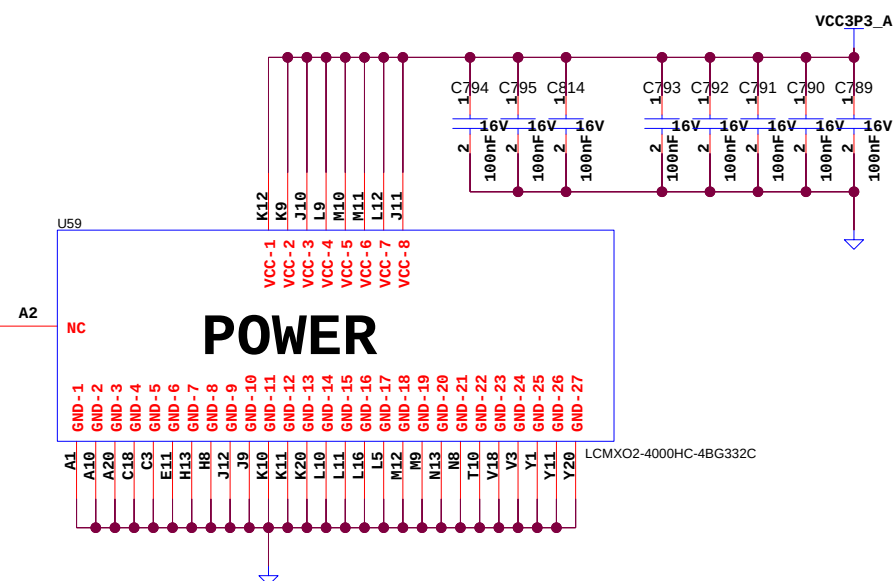
A

A



Will allow testing to toggle between four VCCSA output voltage levels during JTAG test

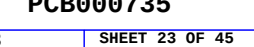
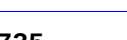
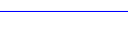
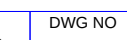
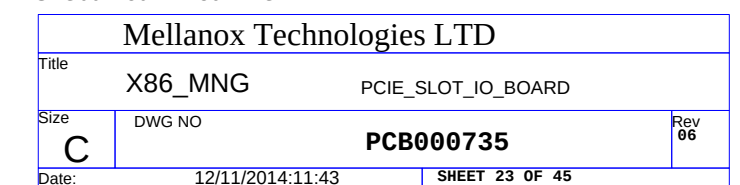




6



6



6

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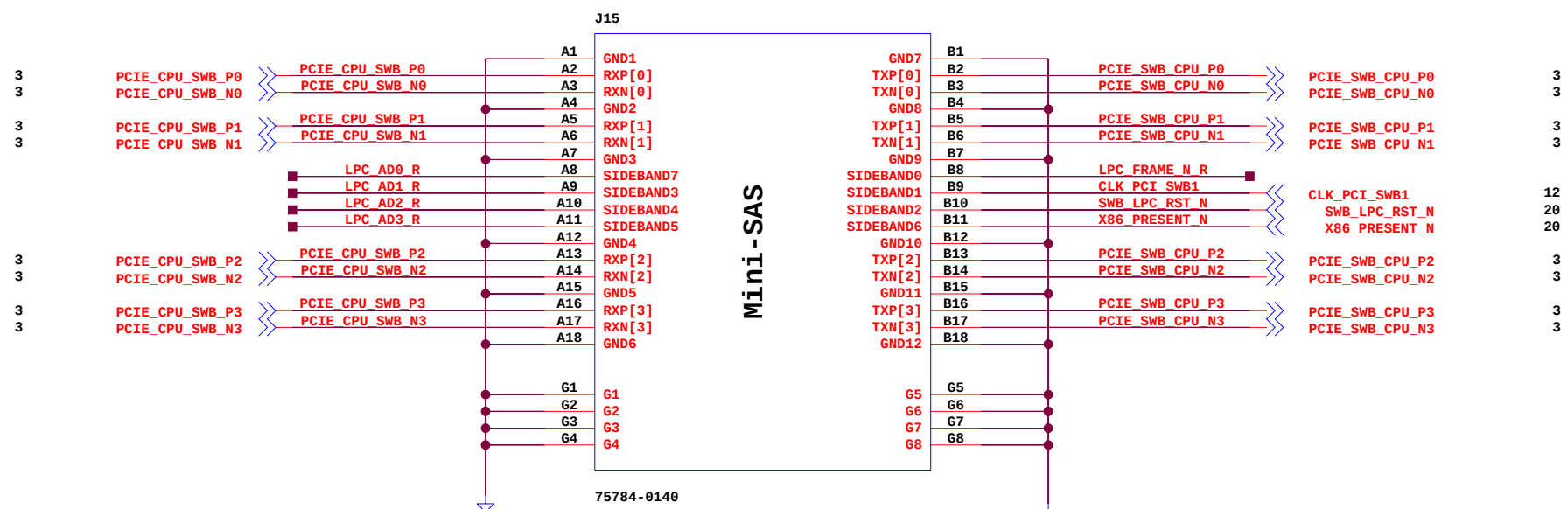
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3

2

1

HS PCIe

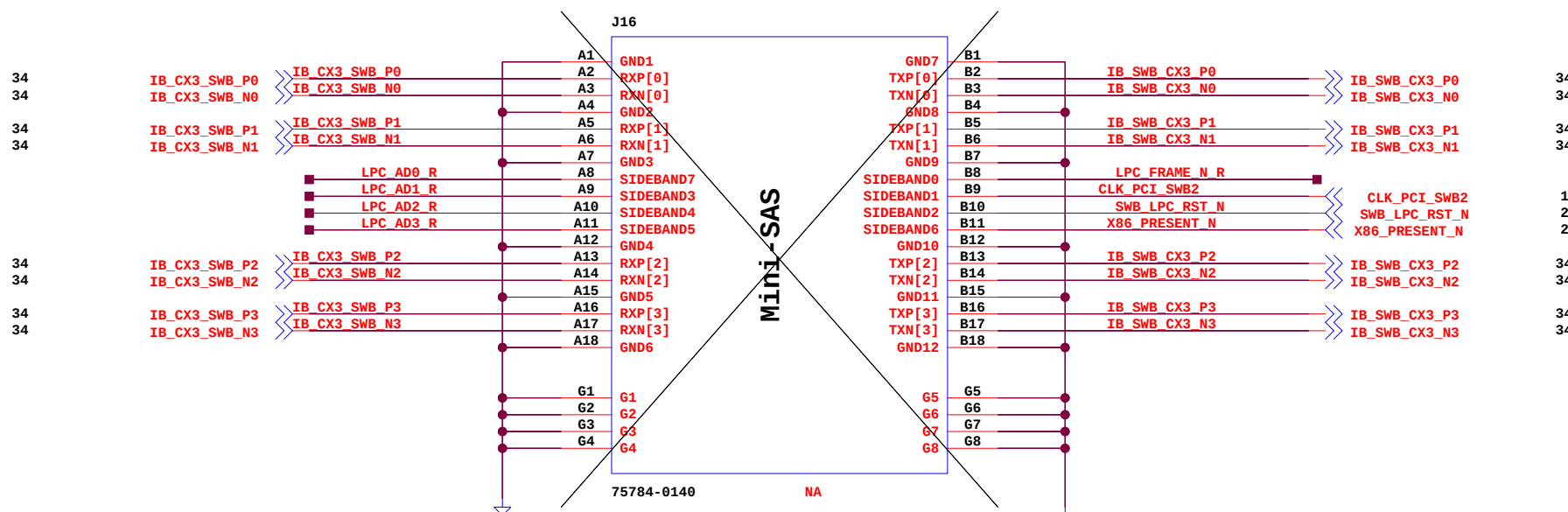


Place Resistors Near HS Connectors

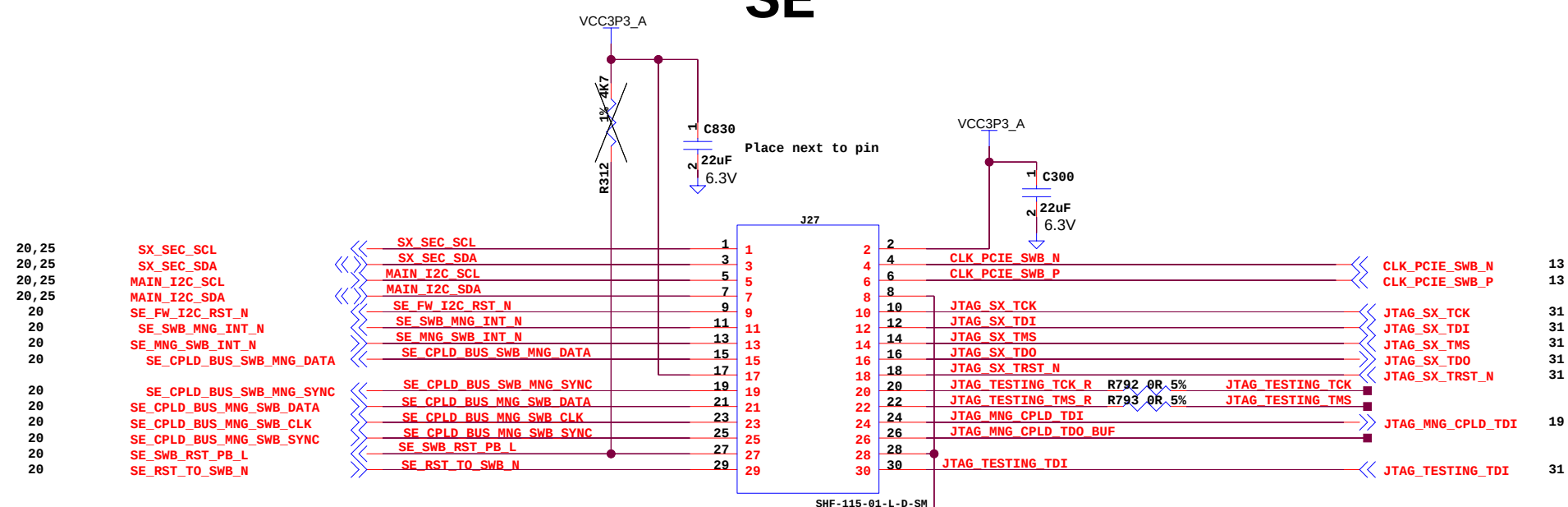


Place Resistors Near HS Connectors

HS IB



SE



Connector pinout changes:

Old Name	New Name
SE_CPLD_BUS_SWB_MNG_SYNC	SWB_PWM
SE_CPLD_BUS_MNG_SWB_SYNC	SWB_TO_MNG_P6
SE_SWB_RST_PB_L	SE_FW_TO_MNG_RST_N (Use to reset FW registers in MNG CPLD)

6

5

4

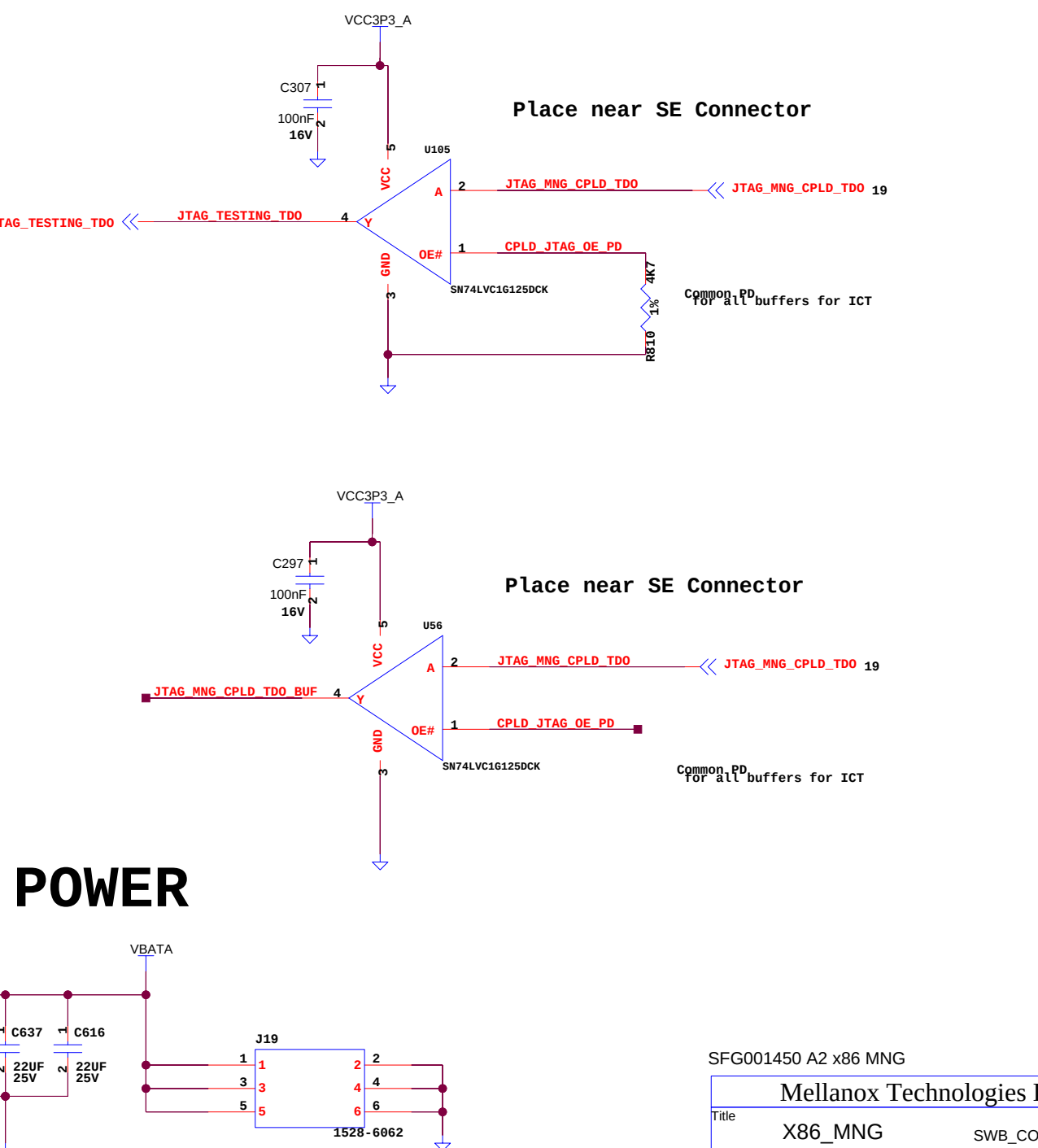
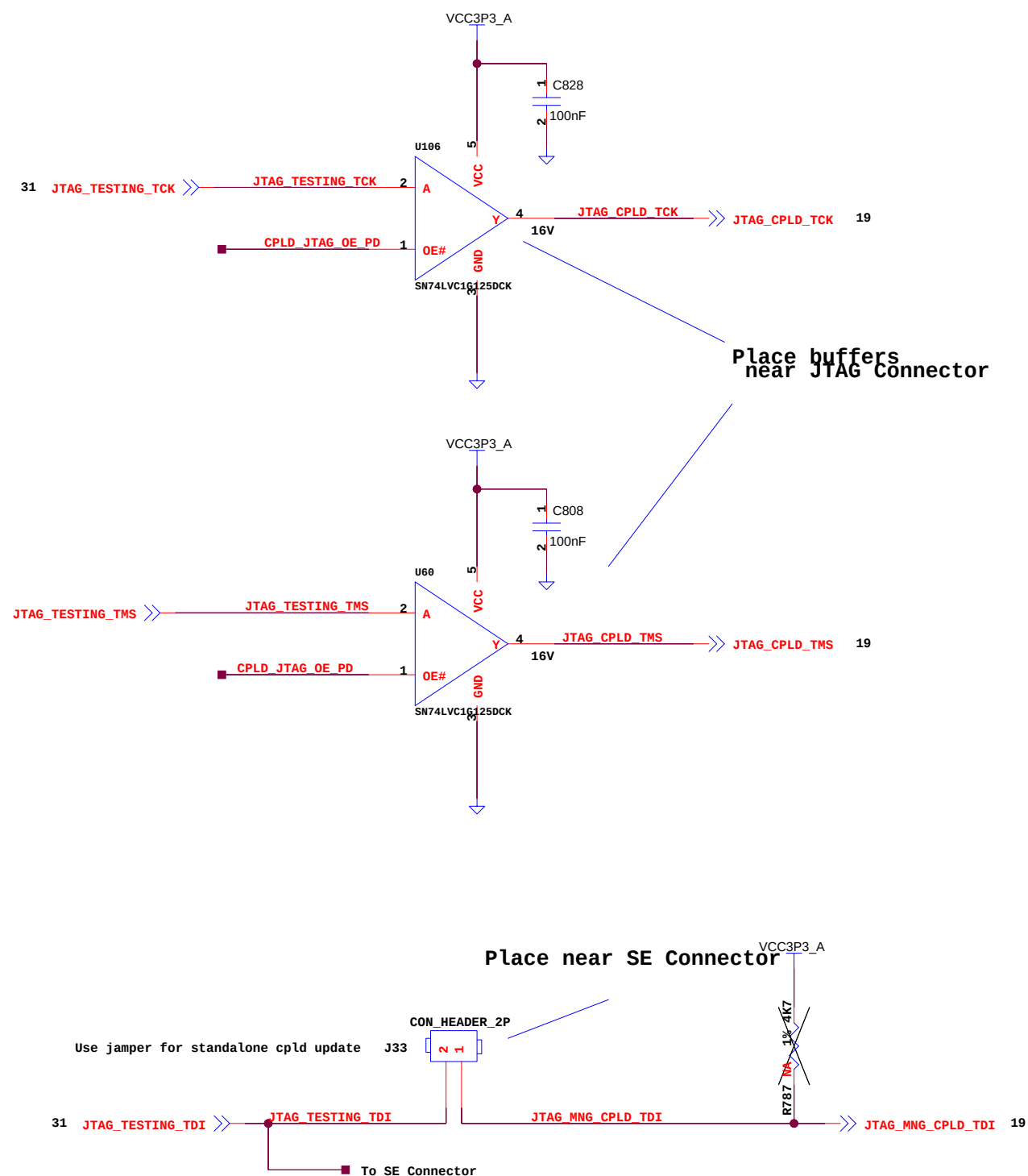
3

2

1

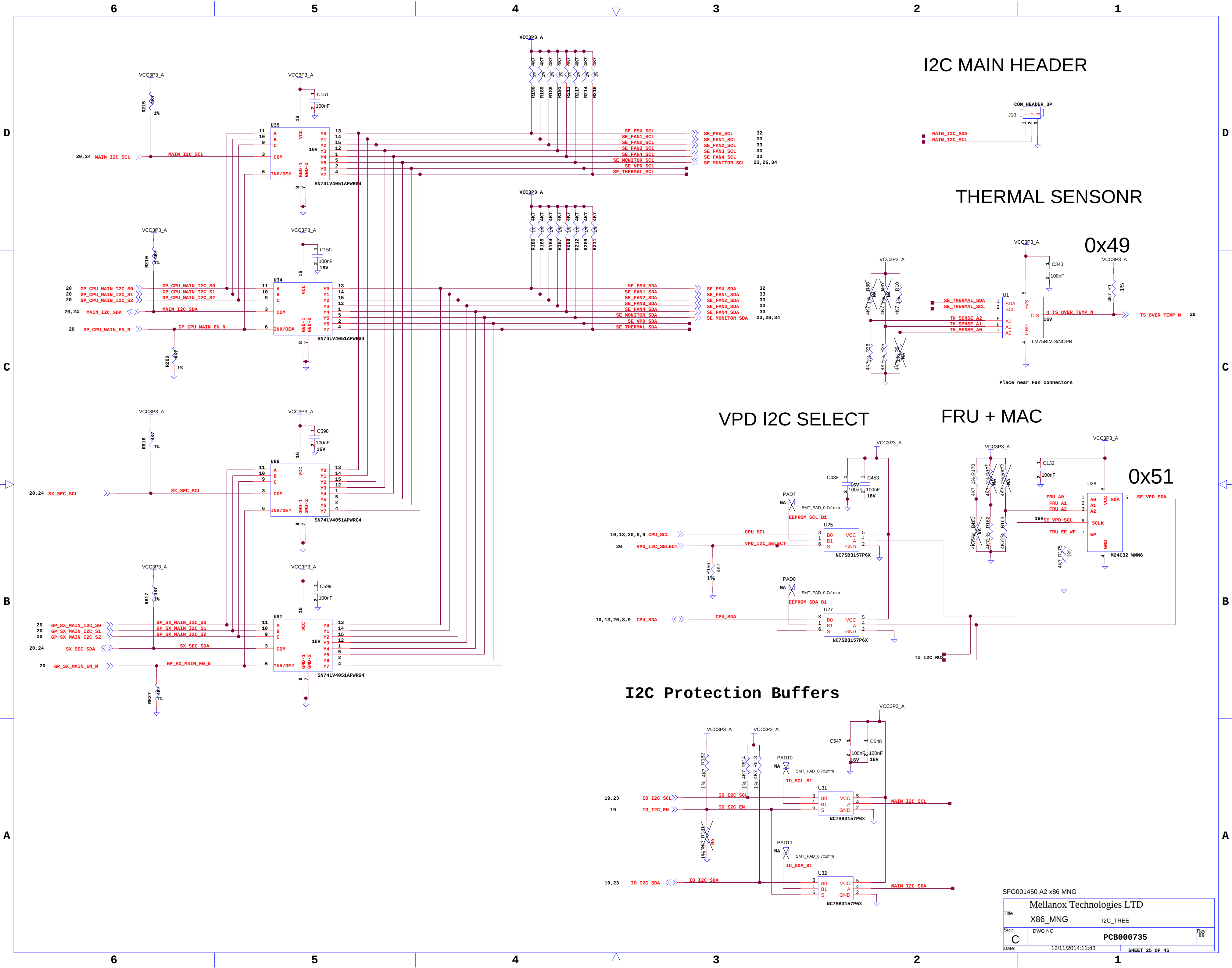
From JTAG CON

To CPLD



SFG001450 A2 x86 MNG

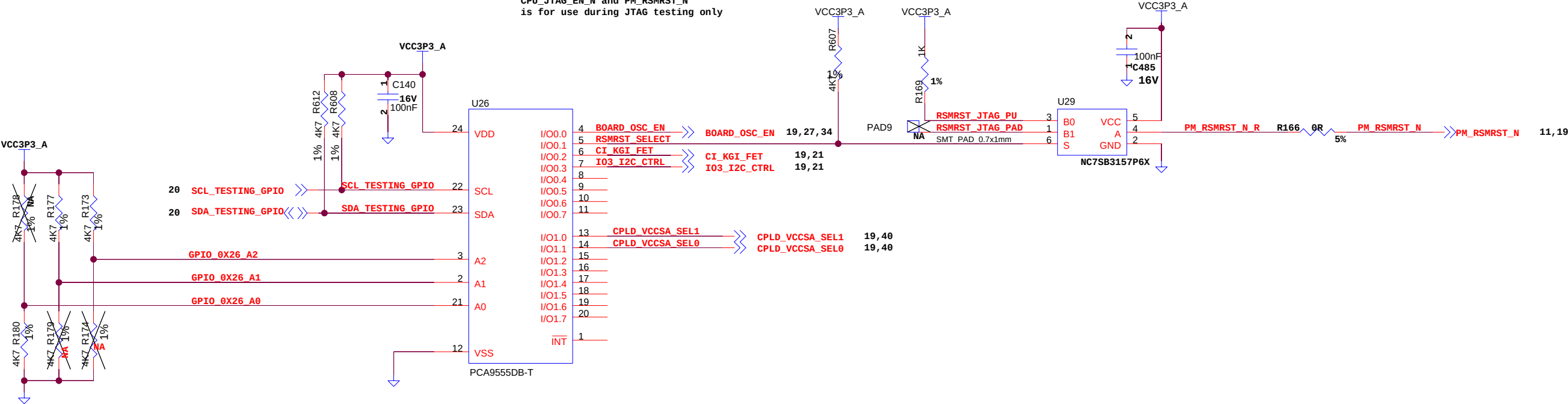
Mellanox Technologies LTD			
Title	X86_MNG		SWB_CONN
Size	DWG NO	PCB000735	Rev 06
Date	12/11/2014:11:43		SHEET 24 OF 45



0x26 TESTING GPIO

At reset the device's ports are inputs with a pull-up to VDD

The GPIO control on the signals
CPU_JTAG_EN_N and PM_RSMRST_N
is for use during JTAG testing only



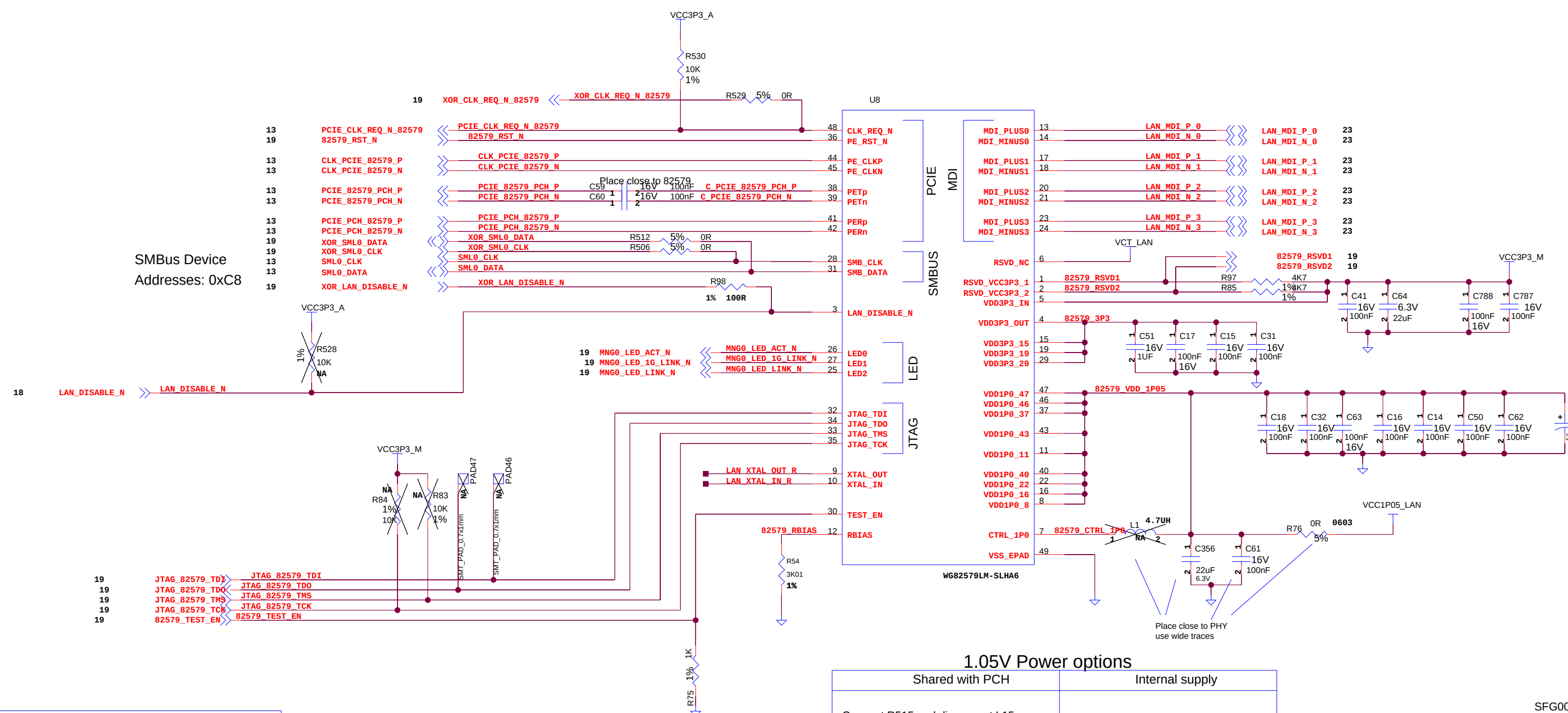
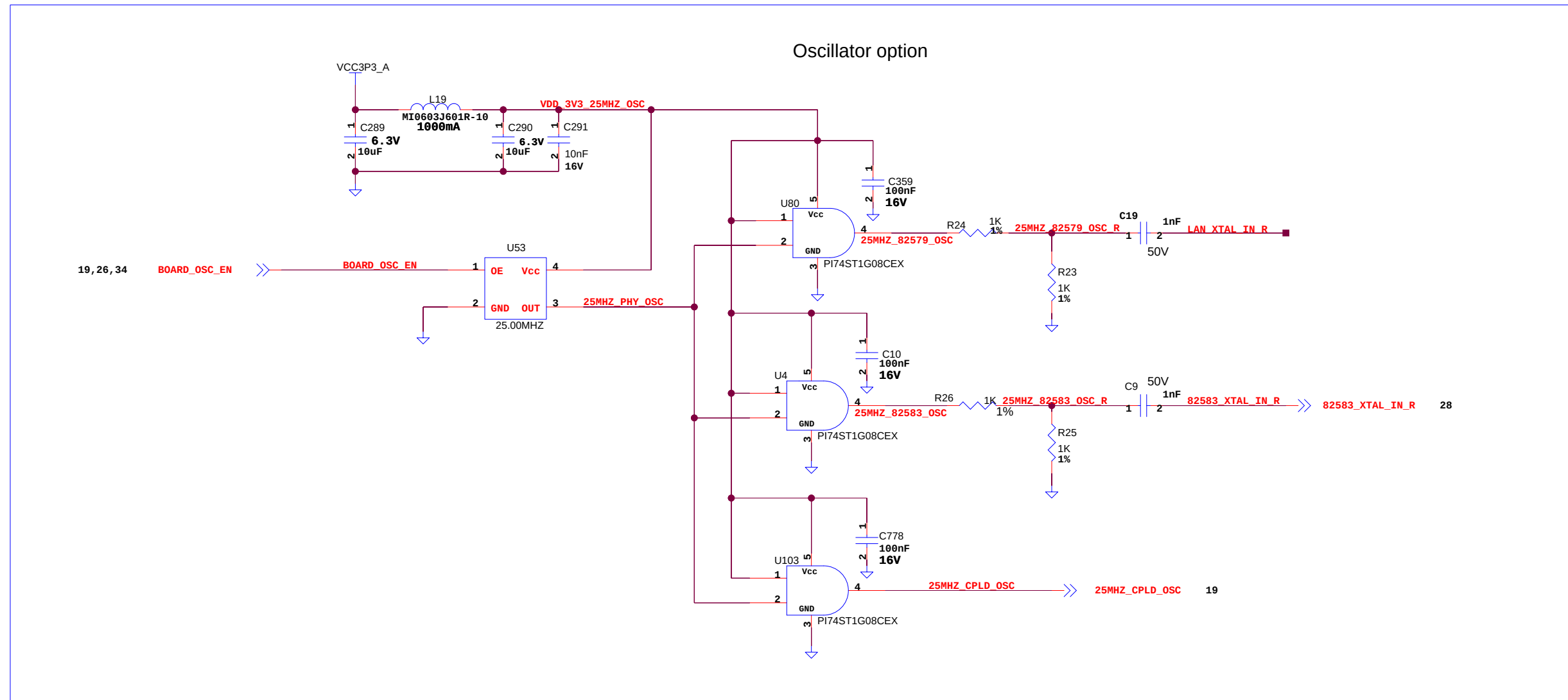
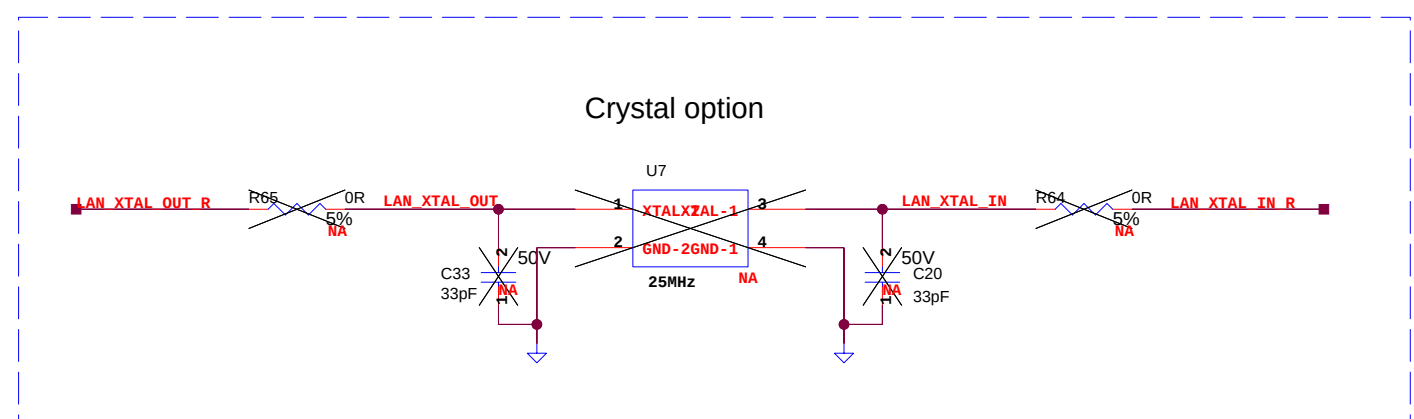
Place near Power supply!

Place caps near A/D

A/D
0x6D

SFG001450 A2 x86 MNG

Mellanox Technologies LTD			
Title	X86_MNG		MONITOR_TESTING
Size	DWG NO	PCB000735	
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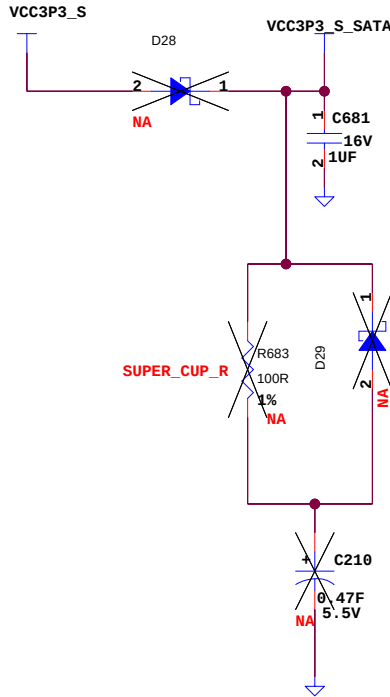
LED Options

All leds are configurable. See table 70 in DS

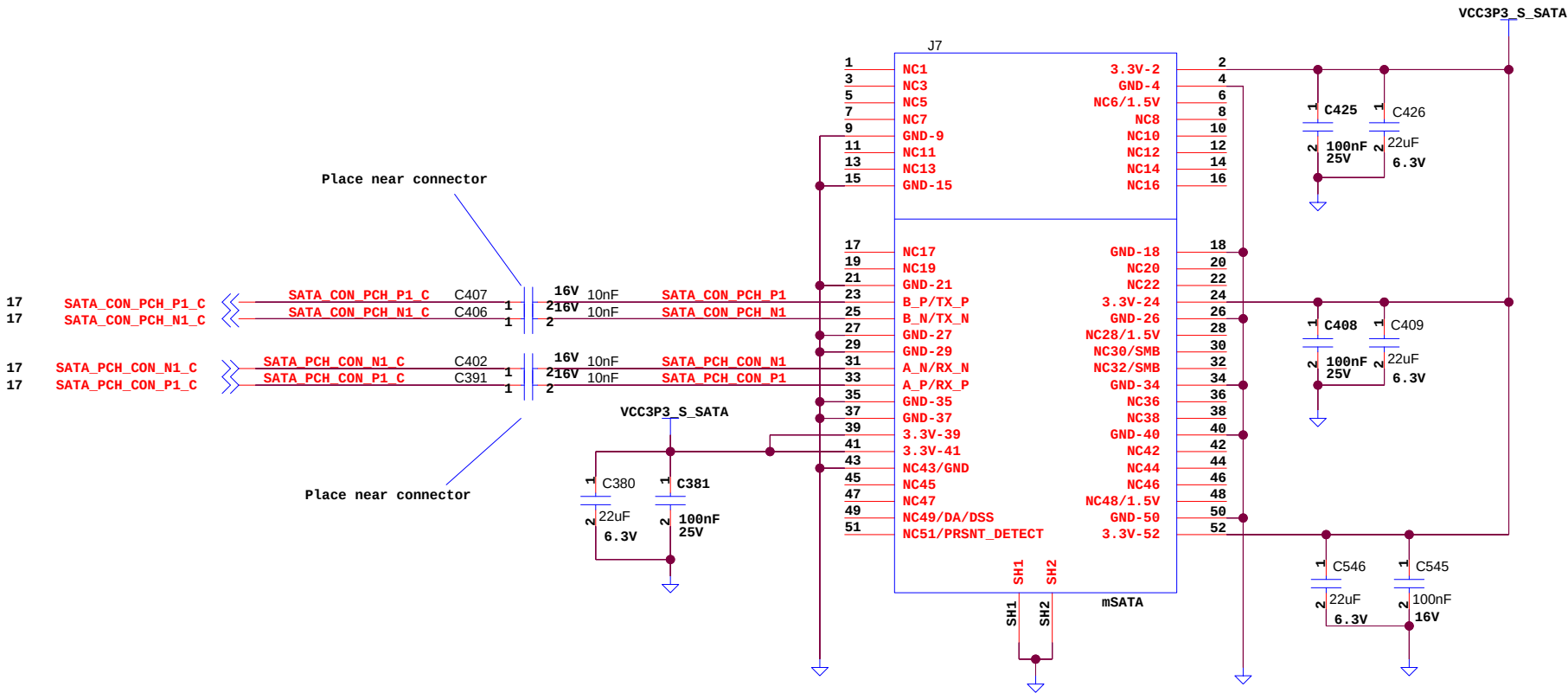
1.05V Power options

Shared with PCH	Internal supply
Connect R515 and disconnect L15 Make sure that PCH's SLP_LAN_N controls both the 3.3V and 1.05V input to 82579	Connect L15 disconnect R515

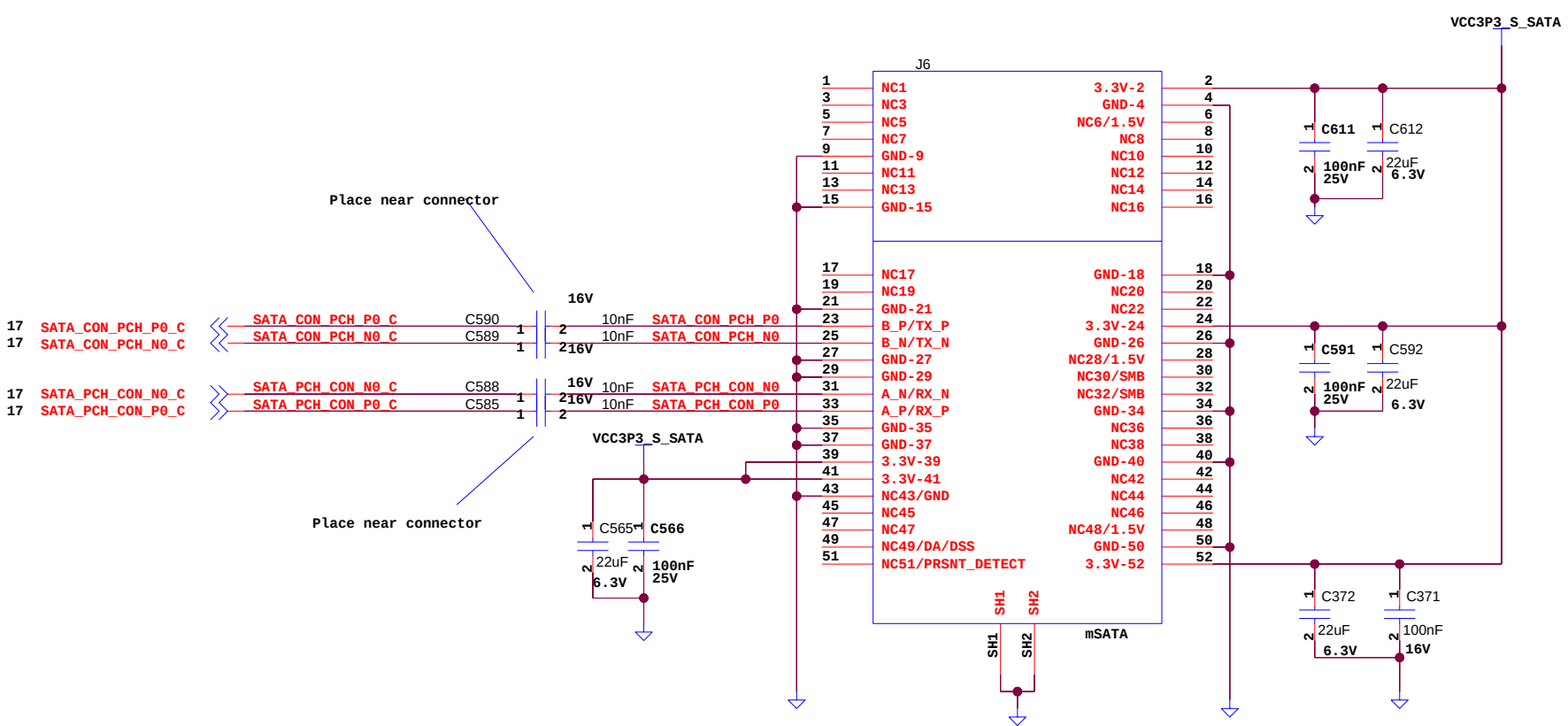
Holdup Capacitor for SATA



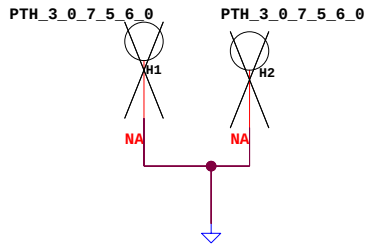
SATA Port 1



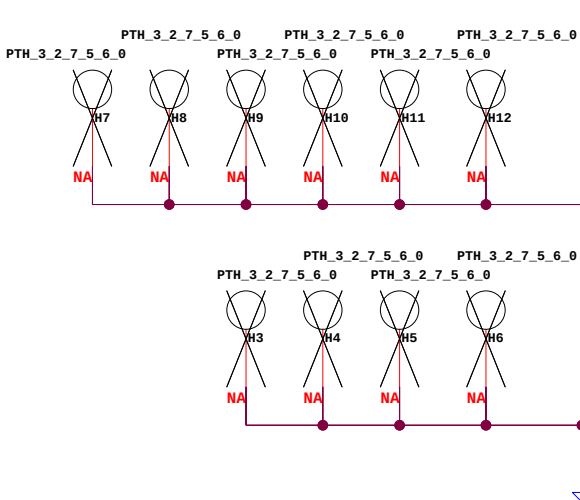
SATA Port 0



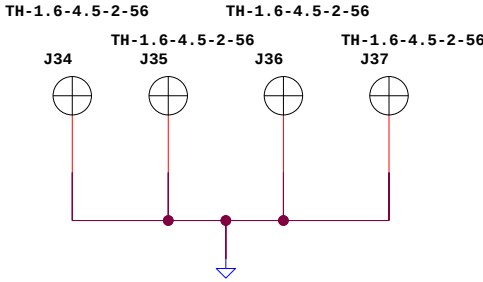
Alignment Pins

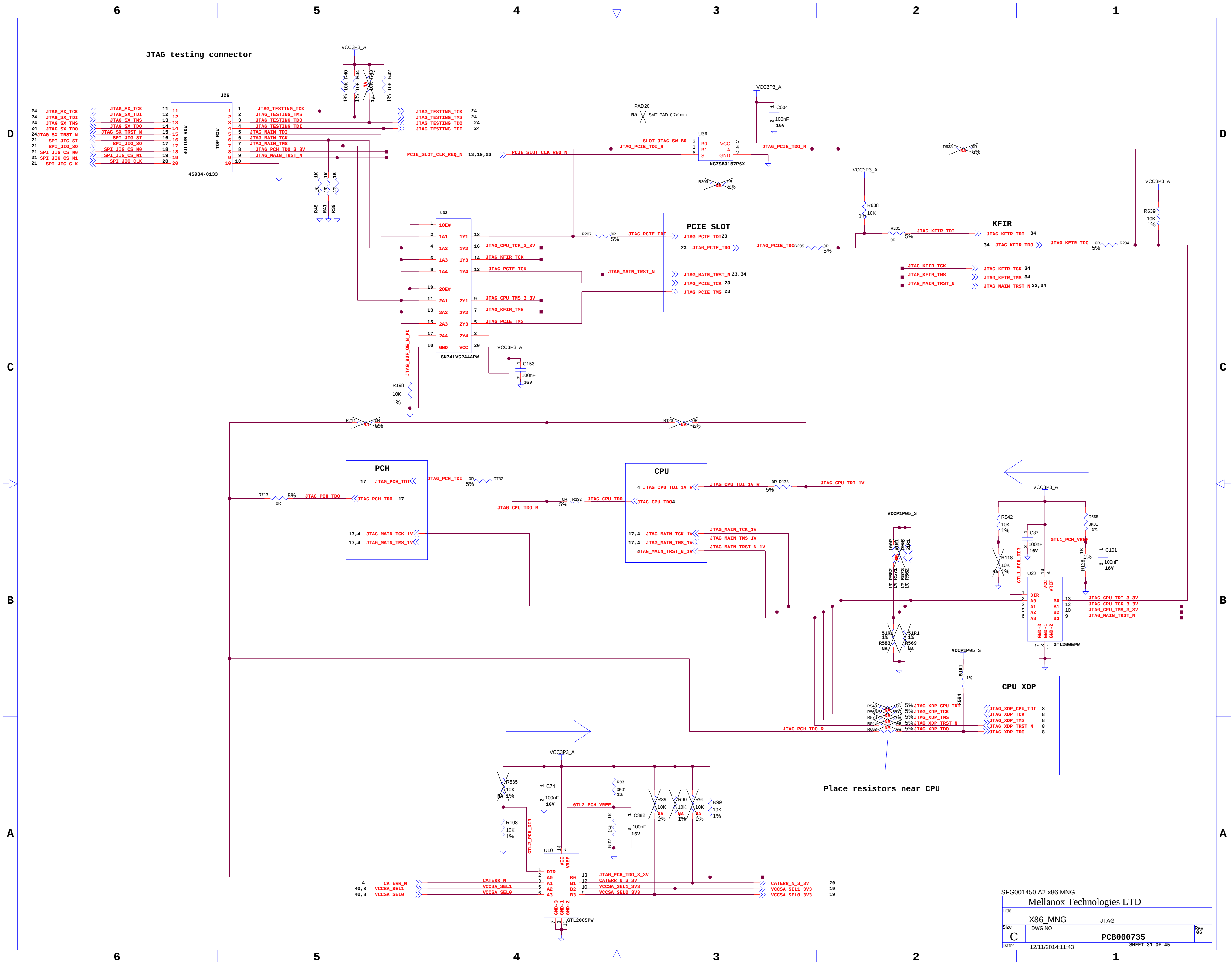


Mechanical Pins

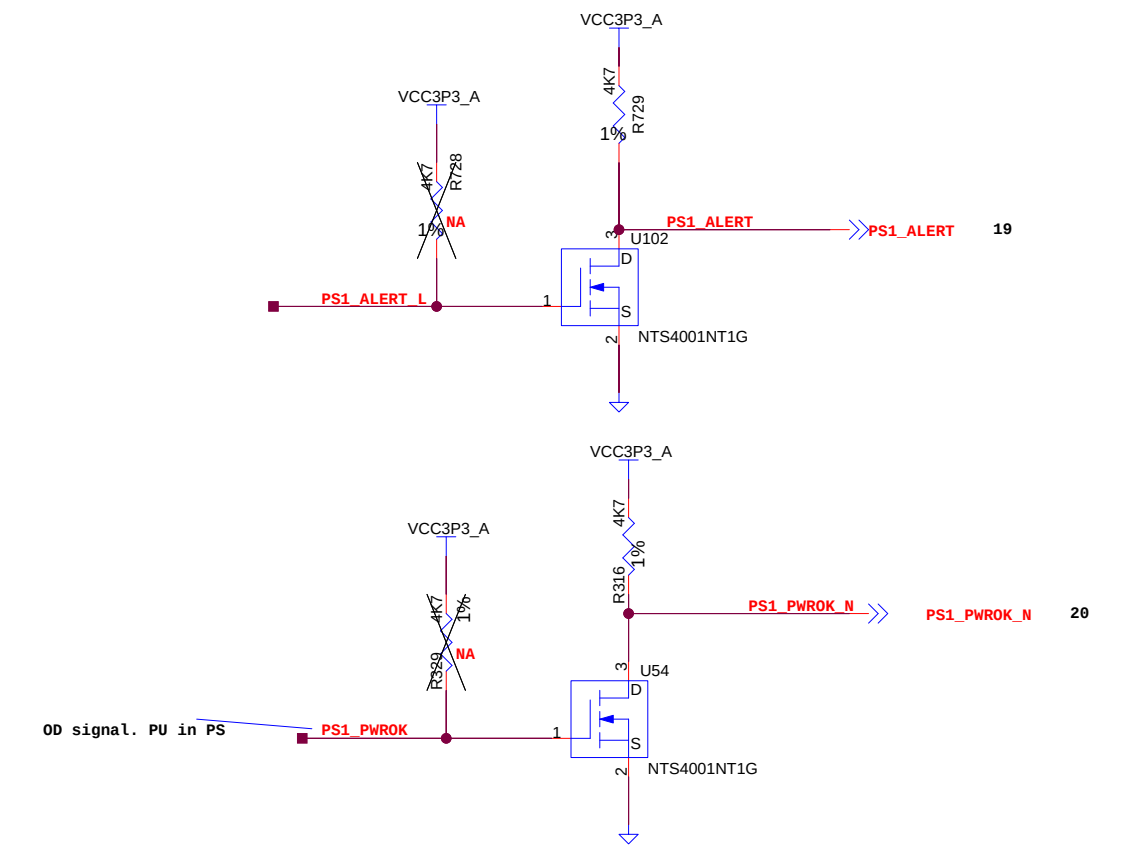
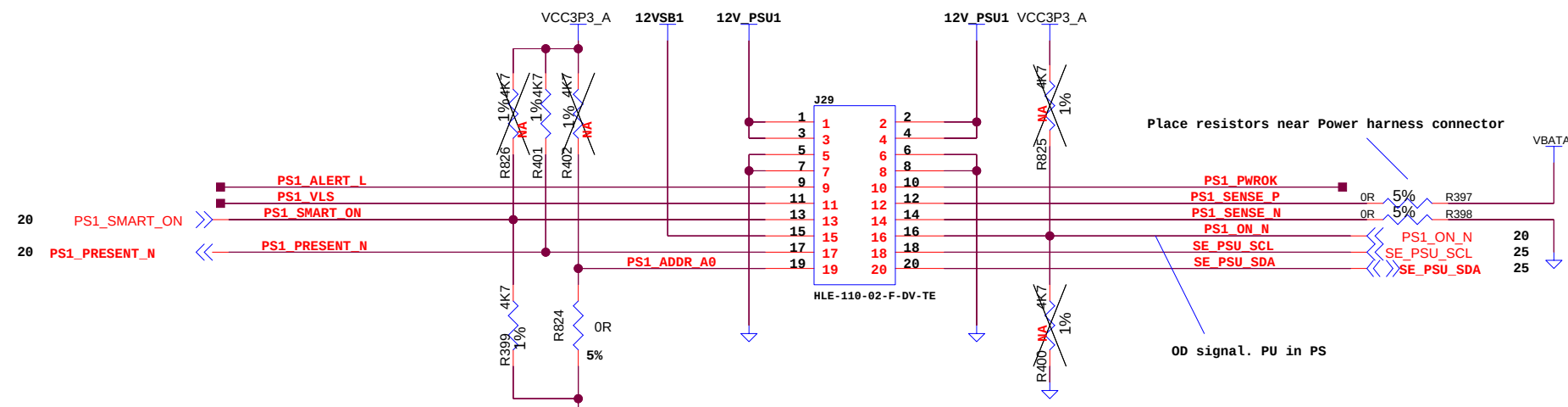
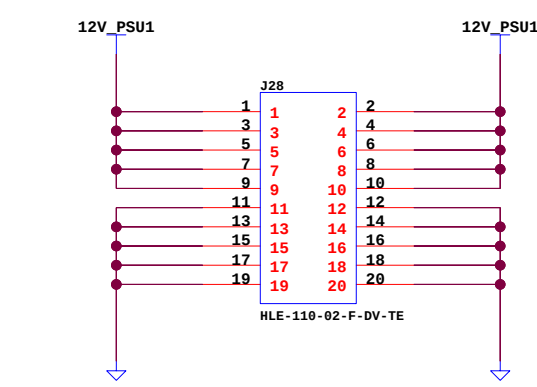


Mount Holes for mSATA

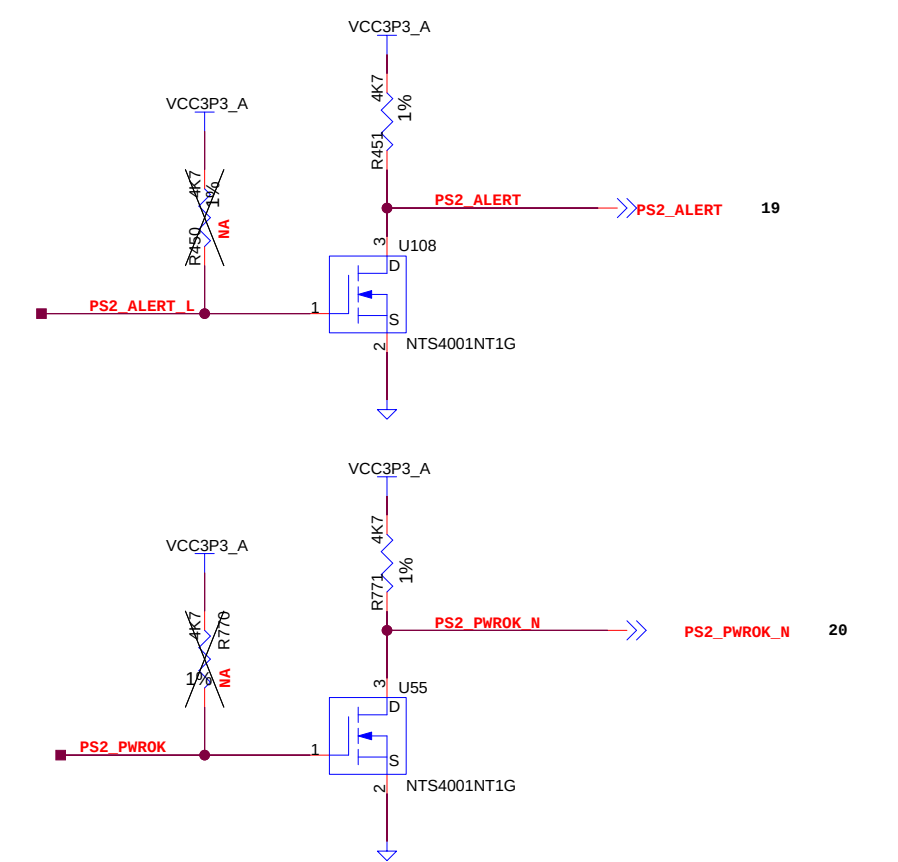
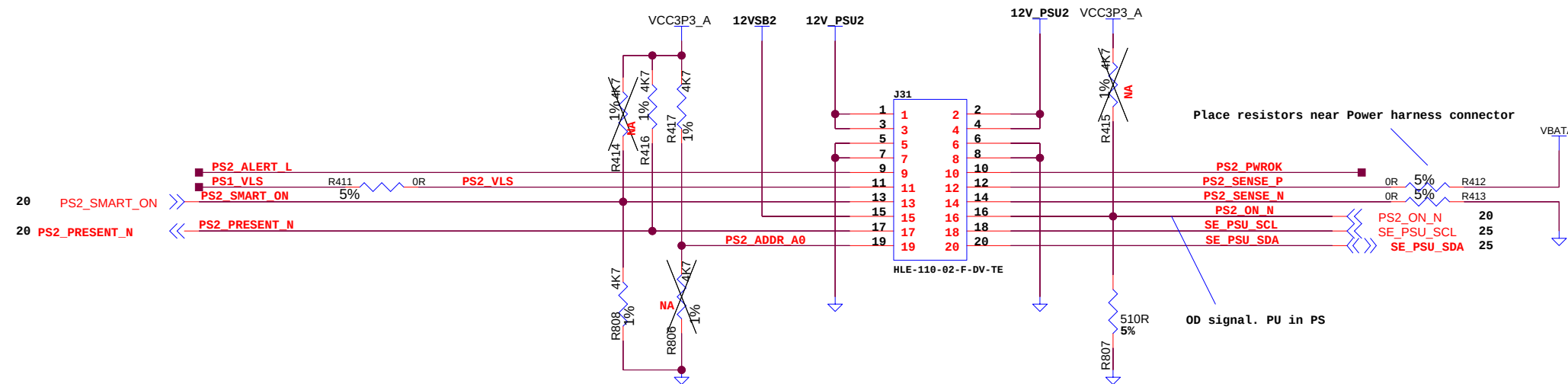
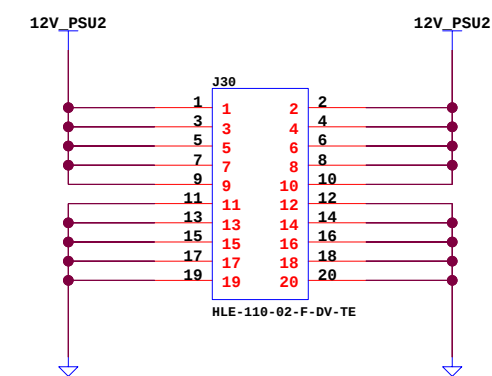




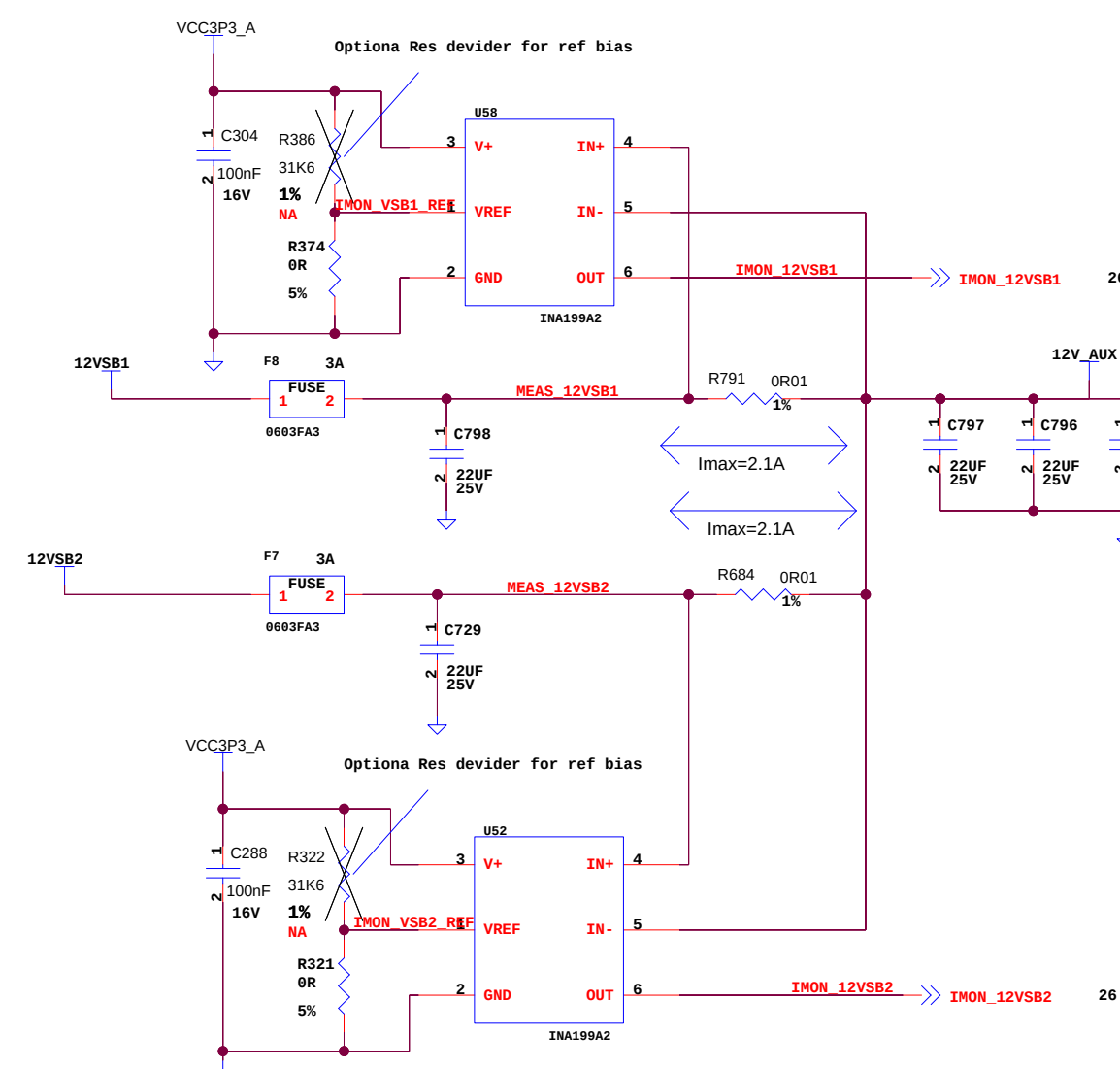
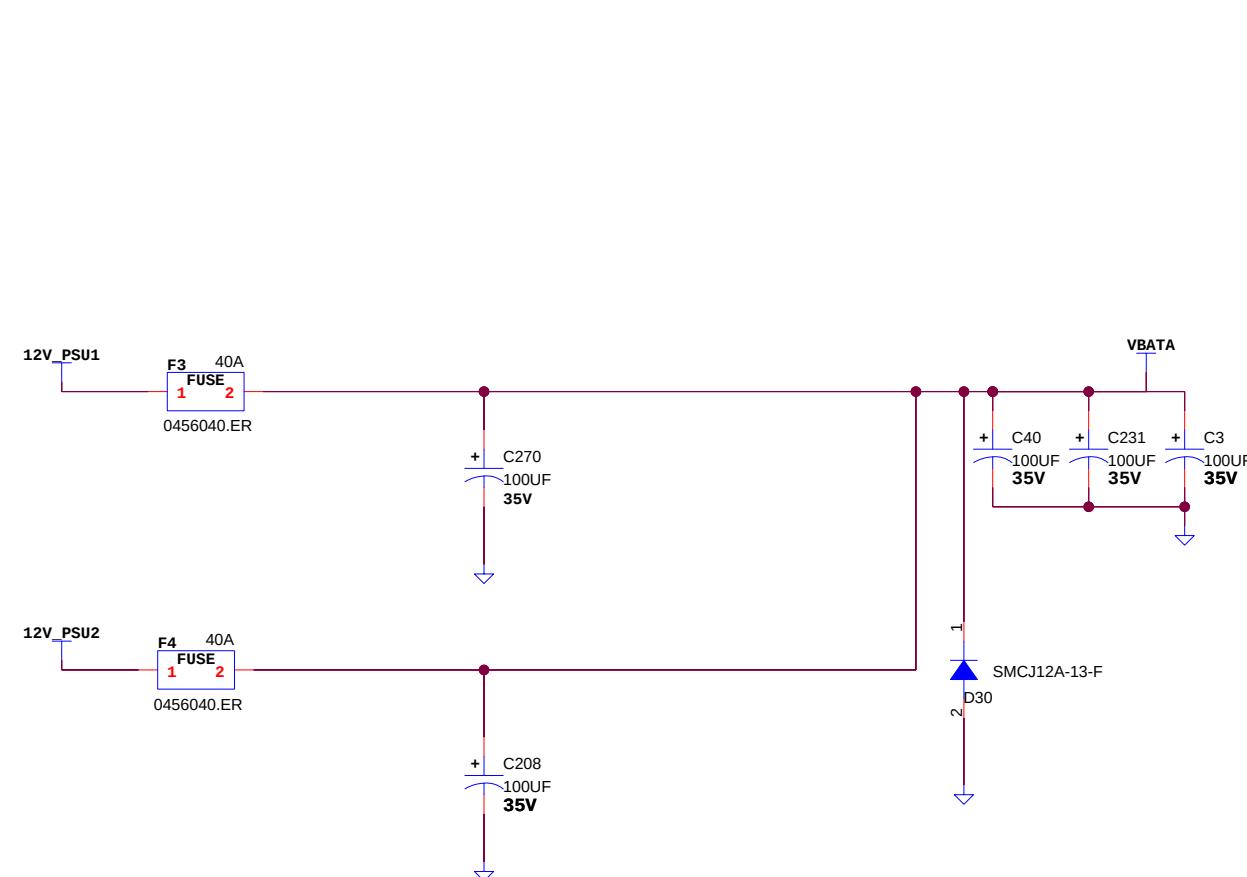
LEFT PS



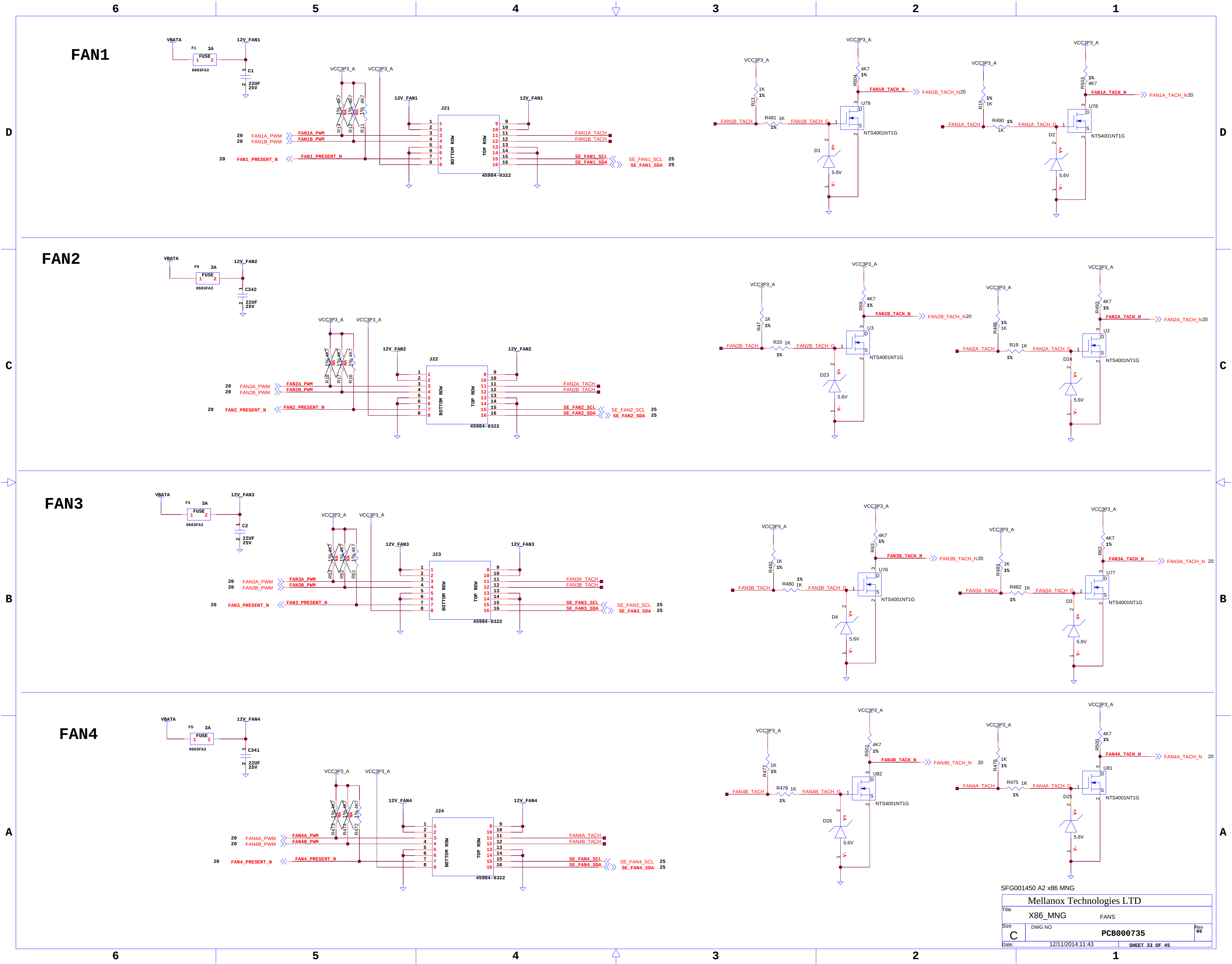
RIGHT PS



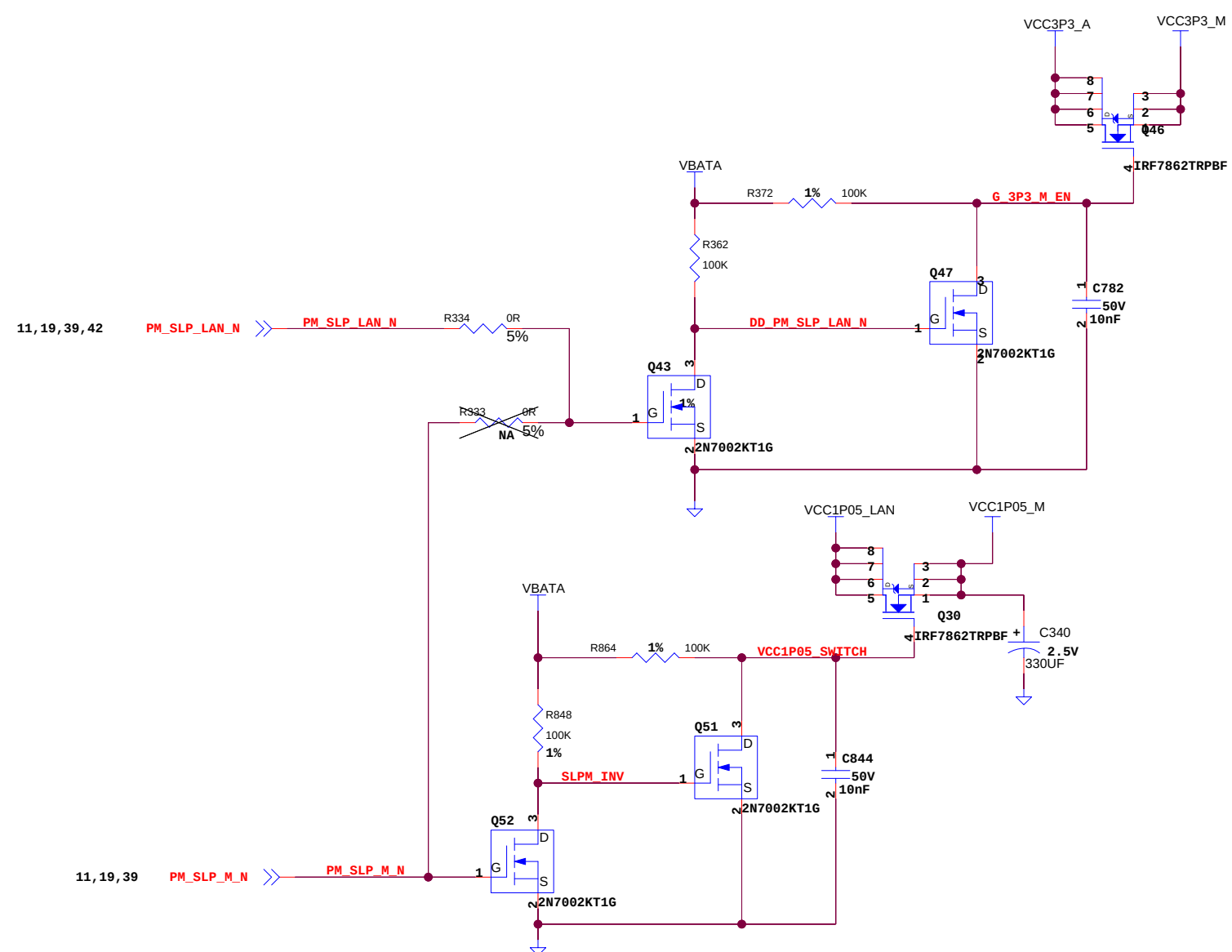
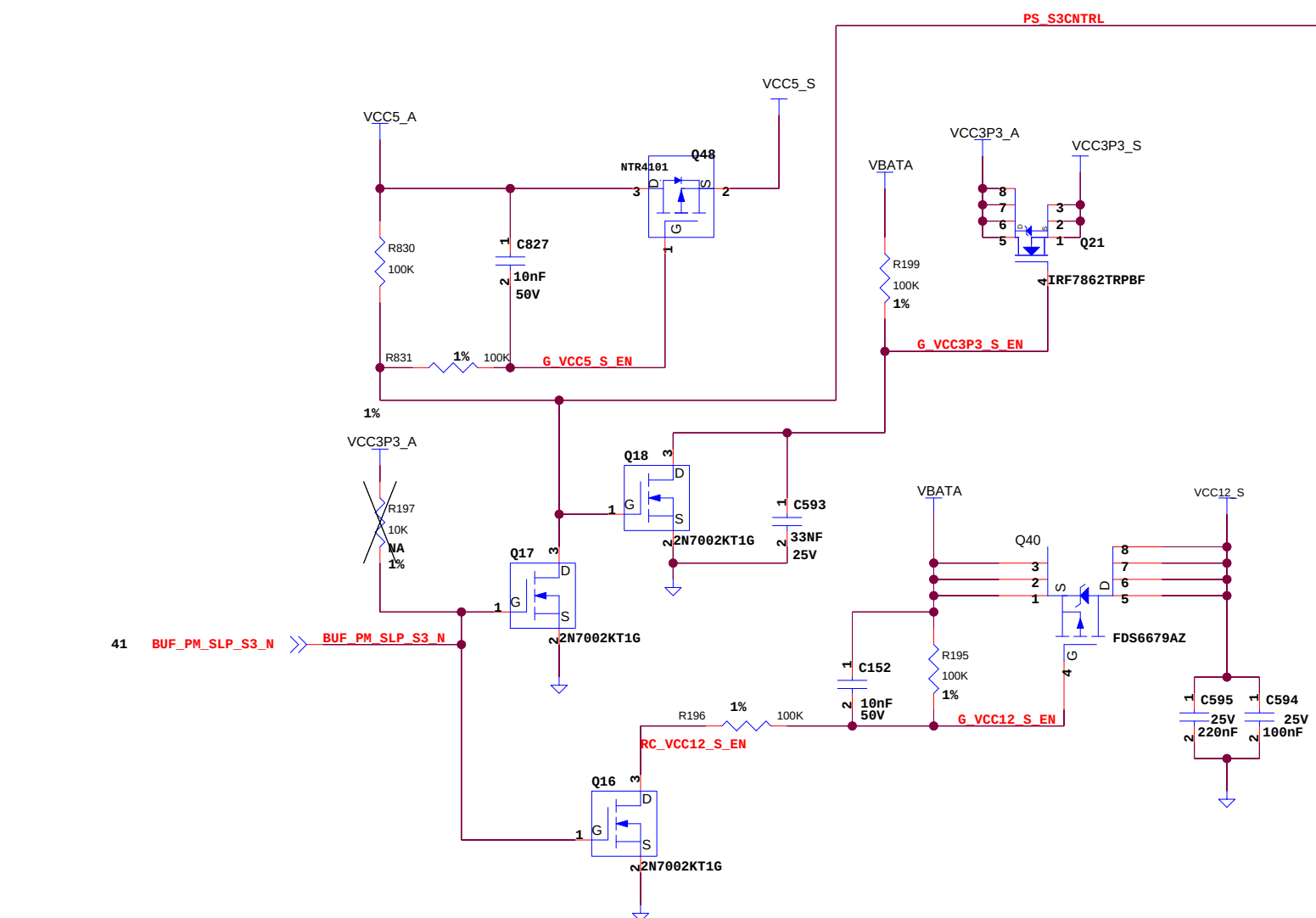
B



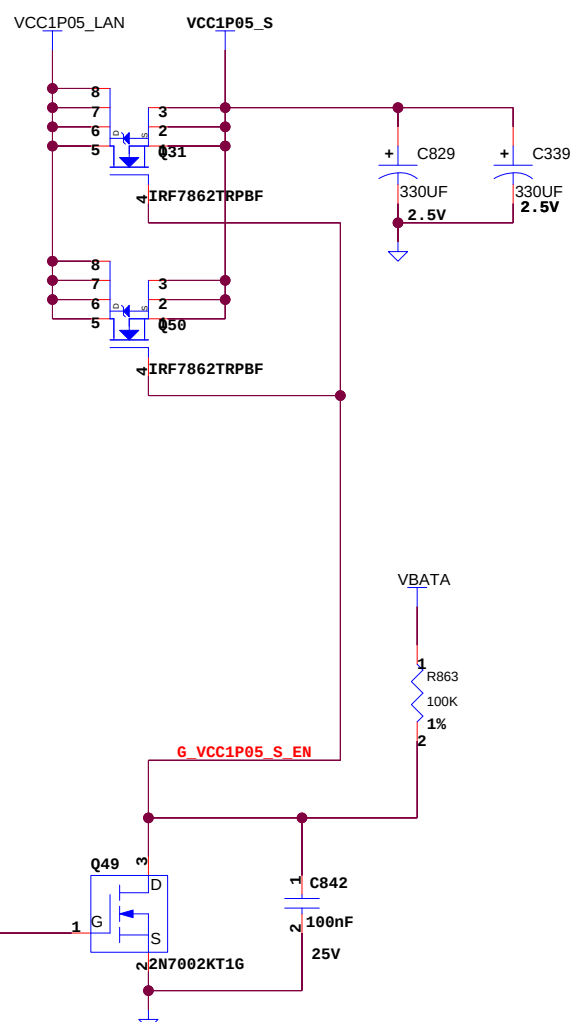
SFG001450 A2 x86 MNG			
Mellanox Technologies LTD			
Title X86_MNG PSU			
Size	DWG NO		Rev 06
C	PCB000735		
Date:	12/11/2014:11:43	SHEET 32 OF 45	



S3 Power

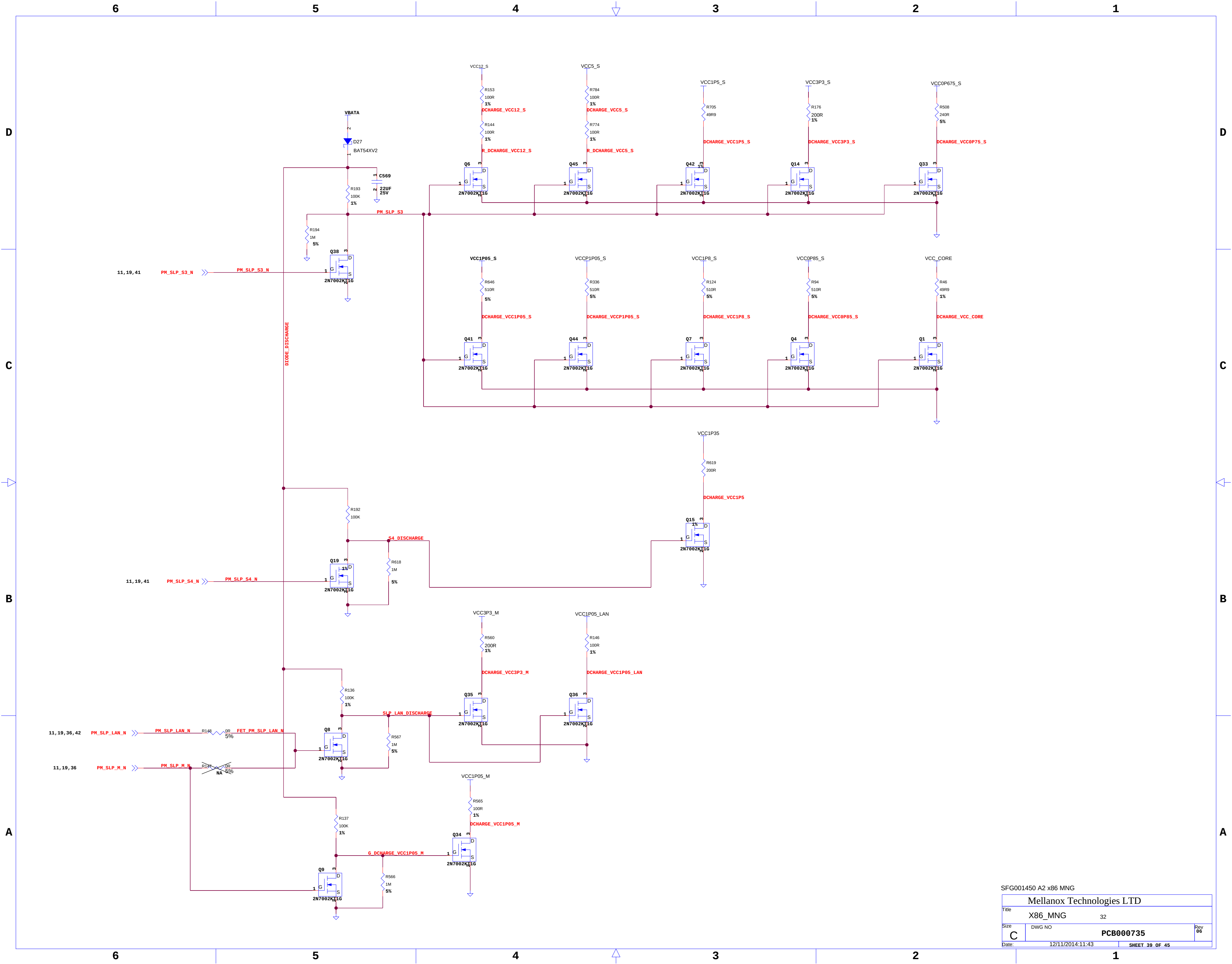


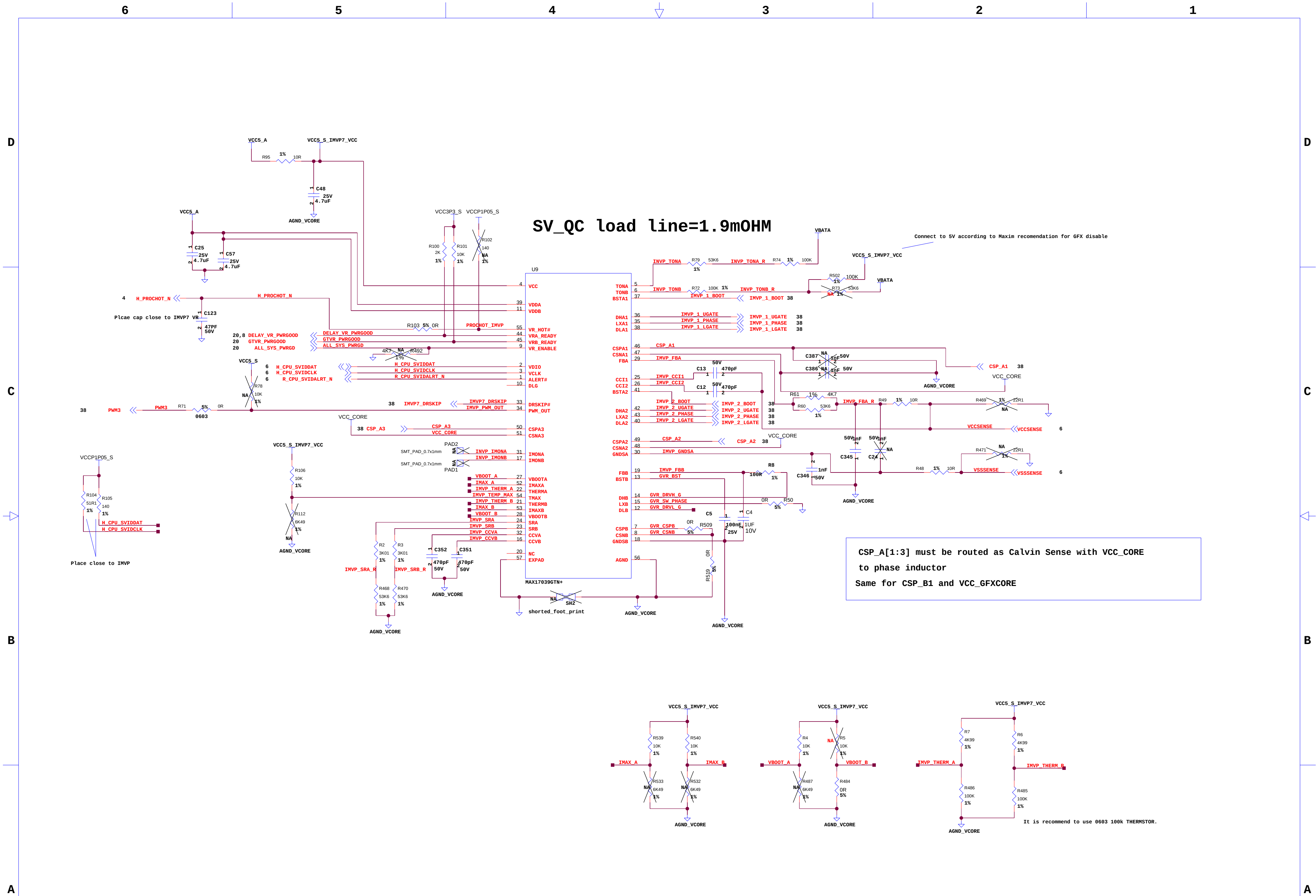
Used to have 4 FETs in paralel.
Reduced to 2 due to placement issues

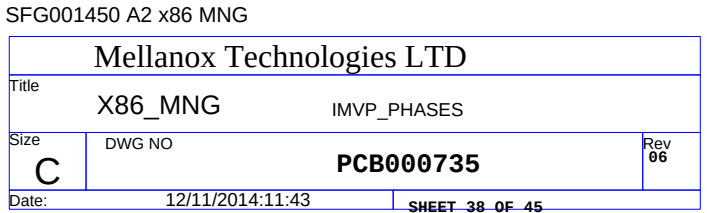


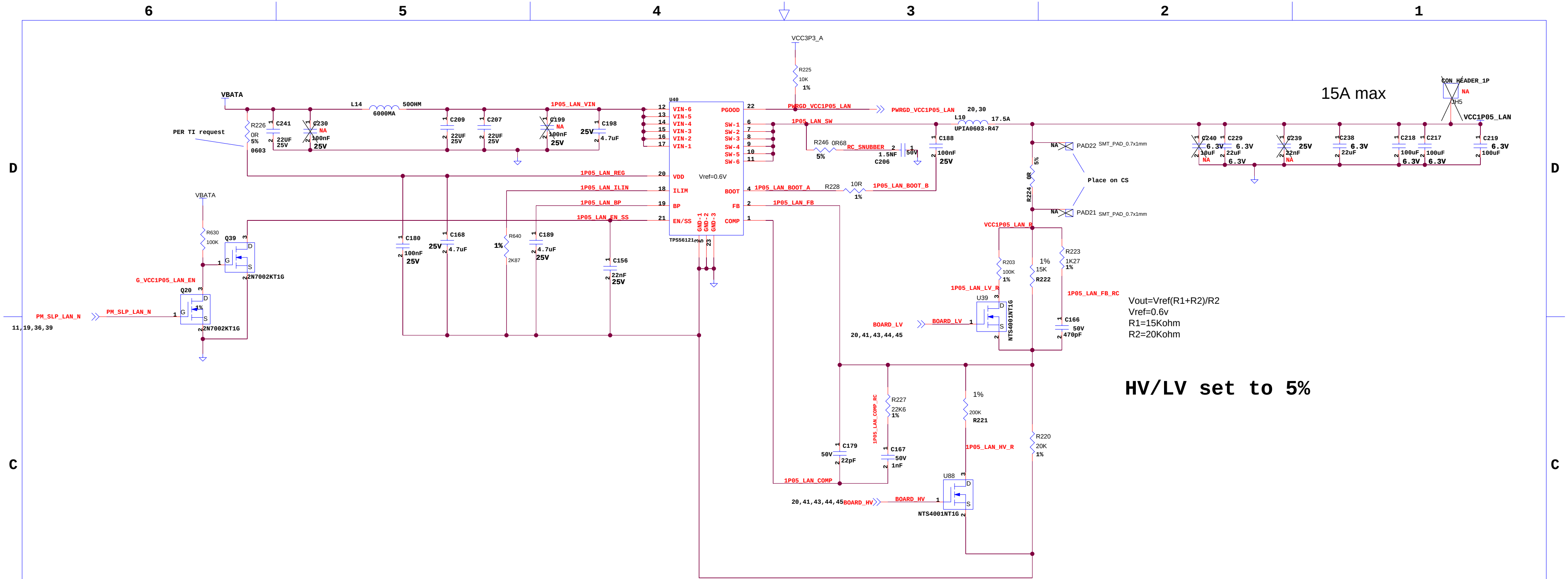
SFG001450 A2 x86 MNG

Mellanox Technologies LTD			
Title	X86_MNG		SLEEP_control
Size	DWG NO	PCB000735	Rev 06
Date:	12/11/2014:11:43	SHEET 36 OF 45	





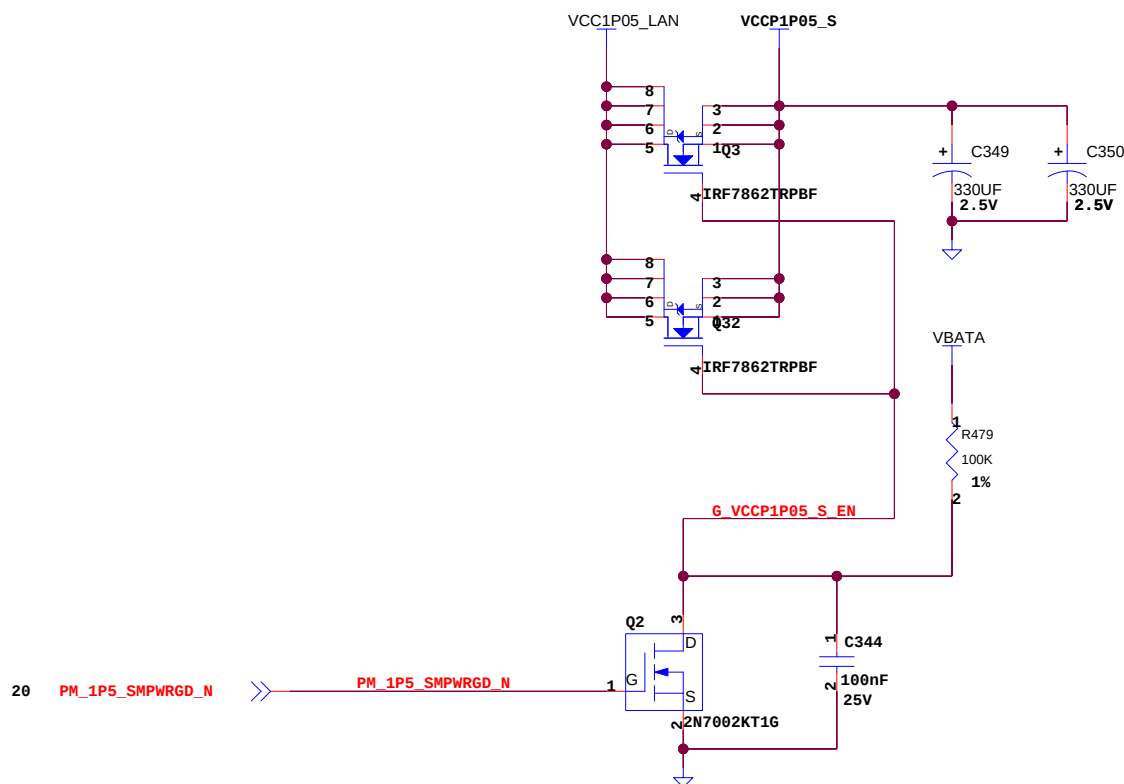




Layout Guidelines:

1. don't separate GNDs, input and output capacitors and the thermal pad and controls GND should be connected to the same GND, the GND plane should be as short as possible
2. Tie the GND pins directly to the thermal pad.
3. Place VIN bypass capacitor as close as possible to VIN pins.
4. Locate the output inductor as close as possible to SW pins with minimal SW plane.
5. BP cap should be located as close as possible to PB pin, Use wide trace.
6. Keep FB trace as far as possible from SW node

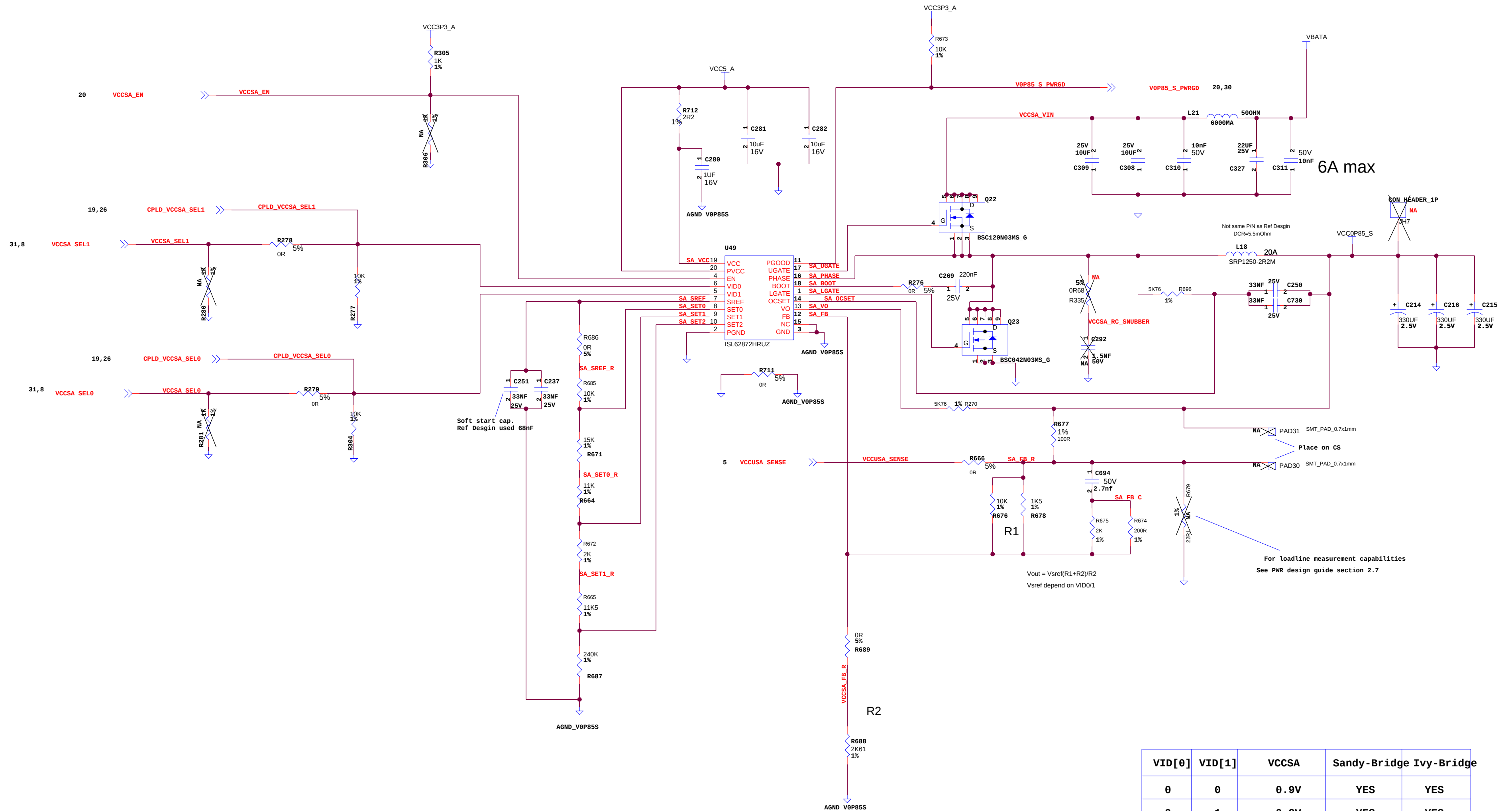
1.05V CPU



SFG001450 A2 x86 MNG

Mellanox Technologies LTD			
Title	X86_MNG		1_05V_LAN
Size	DWG NO	PCB000735	Rev 06
Date:	12/11/2014:11:43		SHEET 42 OF 45

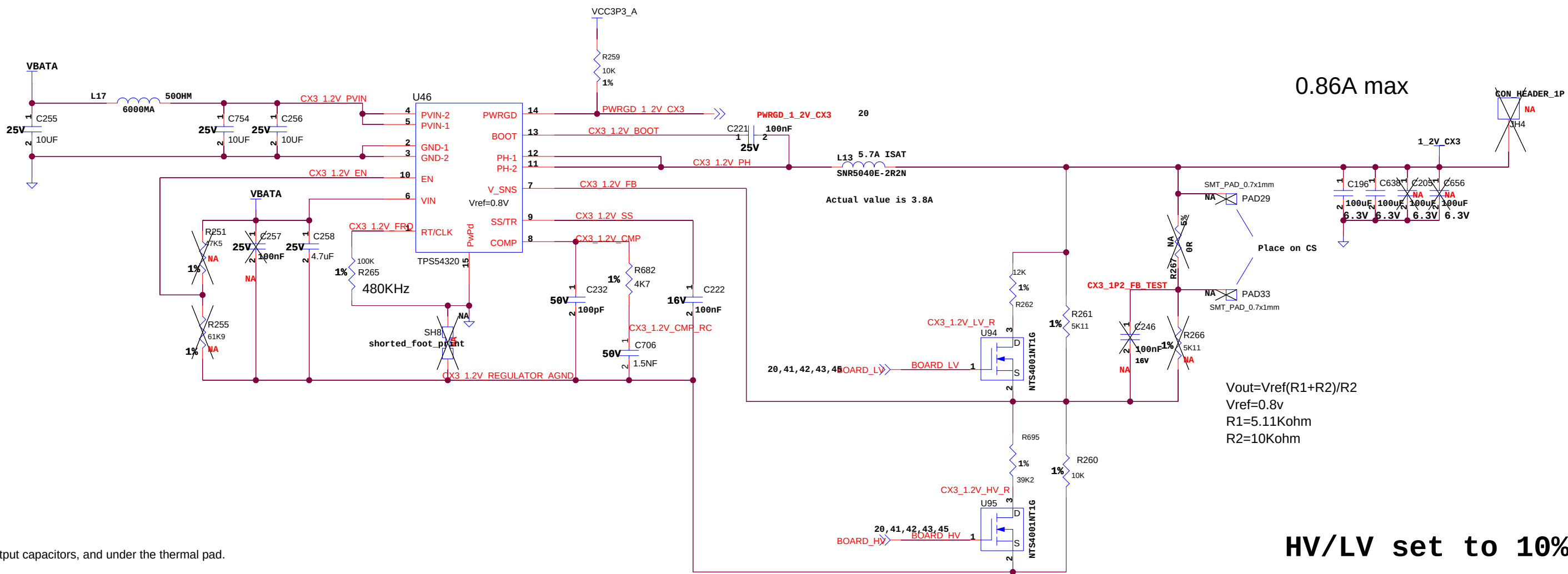
0.85V CPU



VID[0]	VID[1]	VCCSA	Sandy-Bridge	Ivy-Bridge
0	0	0.9V	YES	YES
0	1	0.8V	YES	YES
1	0	0.725V	NO	YES
1	1	0.675V	NO	YES

1. EN pin can float if not used. Use OD output logic if used
3. SS/TR defines the rise time on start up. rise time[ms]=1/3°C

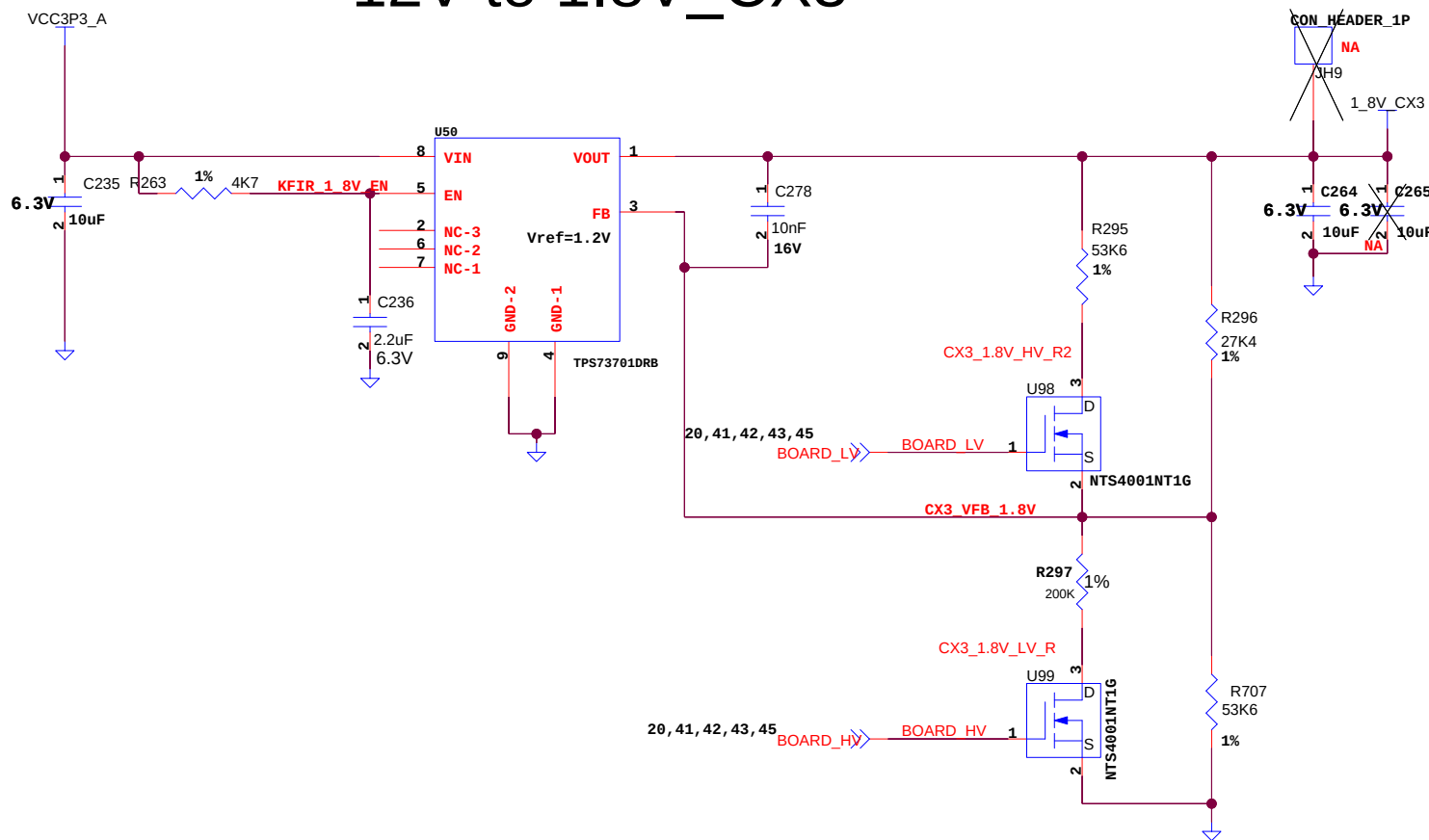
12V to 1.2V POW000075



Layout Guidelines:

1. Connect top layer GND to inner layer GND using vias near input and output capacitors, and under the thermal pad.
2. Tie the GND pins directly to the thermal pad.
3. Place PVIN bypass capacitor as close as possible to PVIN pins.
4. VIN bypass capacitor should be connected to a quite analog GND.
5. Locate the output inductor as close as possible to PH pins with minimal PH plane.
6. The output filter capacitor ground should use the same trace as power ground trace as the PVIN input bypass capacitor. Minimize this trace length. Calculate required width.
7. The small signal components should be grounded to the analog ground path.
8. The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.

12V to 1.8V_CX3



SFG001450 A2 x86 MNG			
Mellanox Technologies LTD			
Title	X86_MNG		KFIR_1_2V_1_8V
Size	DWG NO	PCB000735	Rev 06
Date:	12/11/2014:11:43		SHEET 44 OF 45

2A max

Route in star topology to all destinations
Use min 20mil trace width

25 mil width

15A max

DDR3 VREG
Vout = 1.35V
Fsw = 400K
OCP @ 16A
Iripple = 5A

Route as trace to the bulk caps - Avoid routing near noisy areas

Place resistors close to each other and close to VR

1.8V LDO

Cooling plane:
35mm x 35mm
copper plane
on PS

1.2A max

HV/LV set to 5%

VCC1P5_S LDO

0.17A max

SFG001450 A2 x86 MNG			
Mellanox Technologies LTD			
Title	X86_MNG		DDR3_VR_1.8V_LDO
Size	DWG NO	PCB000735	
C	Date: 12/11/2014:11:43		Rev 06
		SHEET 41 OF 45	

D

- # C

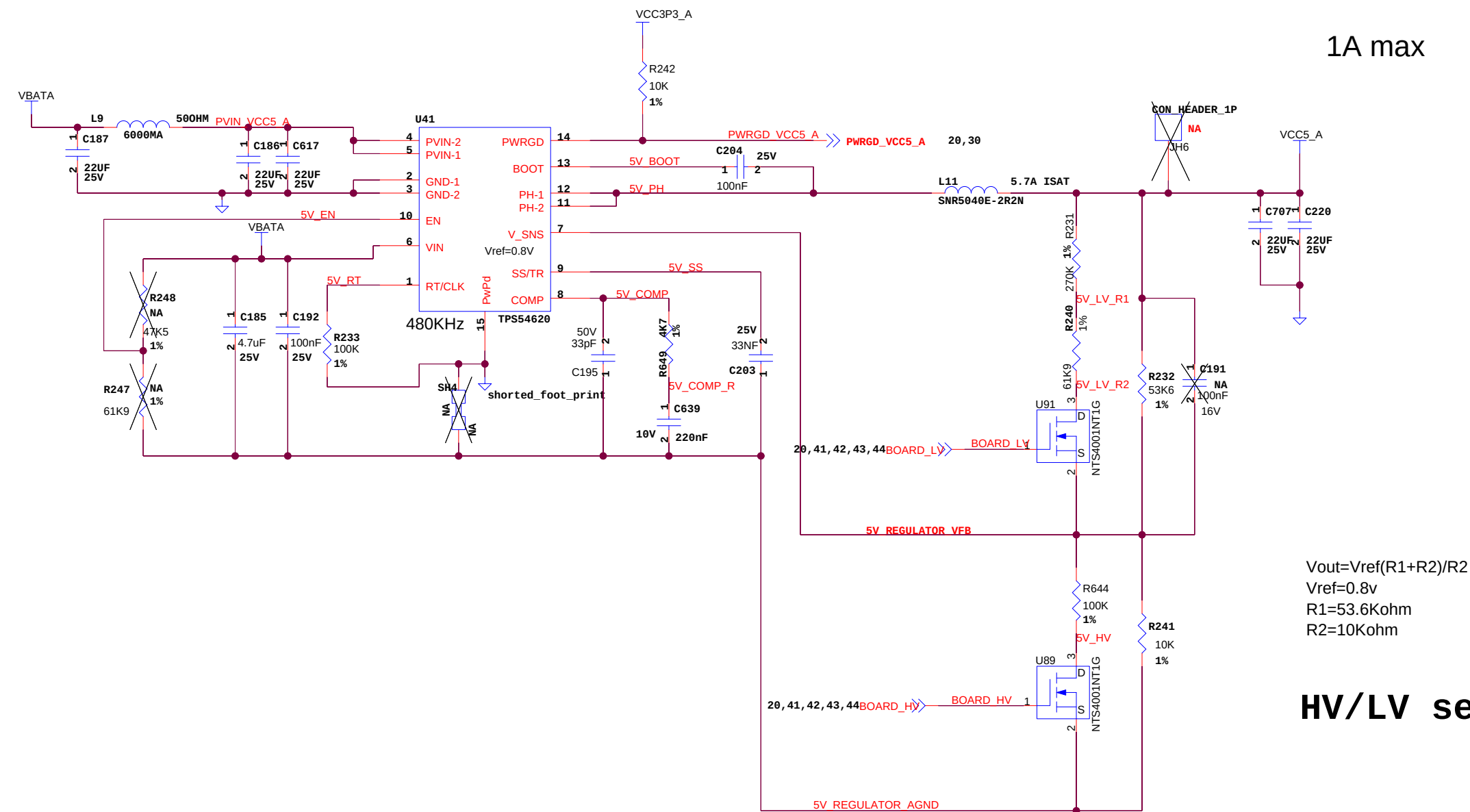
**B**

A

- A**

12V to 5V - POW000059

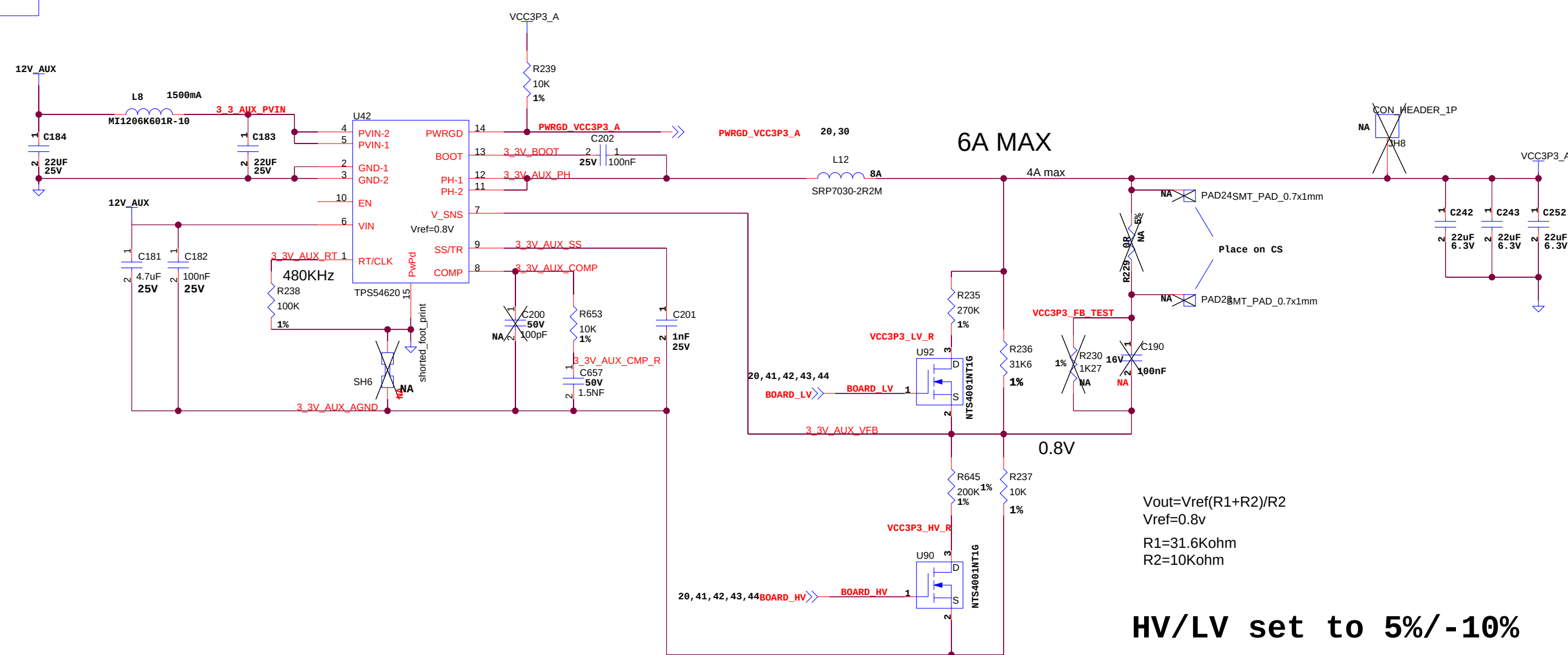
1A max



12V to 3.3V - POW000059

VCC3P3_A is fed from 12VSB - always ON!

MAX current from 12V_AUX is 2.1A



Layout Guidelines:

1. don't seperate GNDs, input and output capacitors and the thermal pad and controls GND should be connected to the same GND , the GND plane should be as short as possible
2. Tie the GND pins directly to the thermal pad.
3. Place VIN bypass capacitor as close as possible to VIN pins.
4. Locate the output inductor as close as possible to SW pins with minimal SW plane.
5. Keep FB trace as far as possible from SW node

SFG001450 A2 x86 MNG

Mellanox Technologies LTD			
Title	X86_MNG		3_3v_5v
Size	DWG NO	PCB000735	Rev 06
Date:	12/11/2014:11:43		SHEET 45 OF 45